CONSUMER INTEGRATED CIRCUIT HANDBOOK

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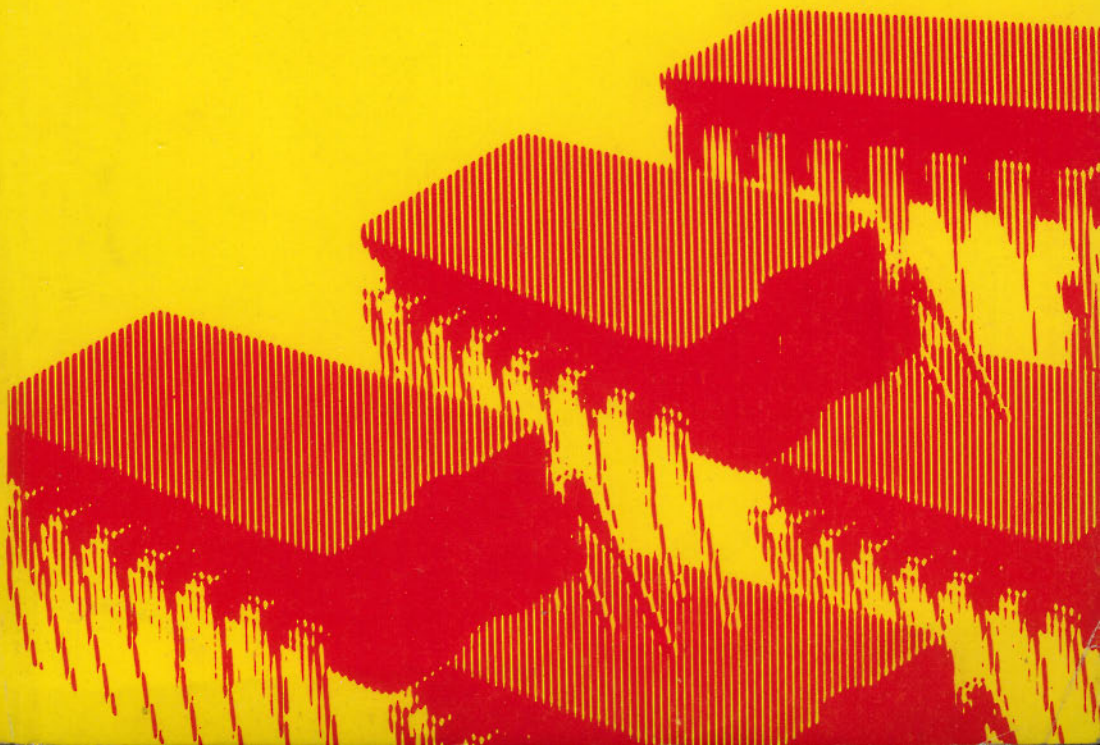

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Designed and produced by Peter Wigens Consultants

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Contents

Product index

		PAGE
ML2001	Teletext/Viewdata control interface	13
ML2040	On-screen display circuit	10
SL439	IF filter preamplifier	13
SL470	BCD decoder—varicap diode driver	13, 75
SL480	Infra-red detector preamplifier	12, 77
SL490	32 code remote control transmitter	12, 81
SL491	32 code remote control transmitter	12, 85
SL901	Colour decoder matrix circuit	13
SL917	Colour decoder combination	13
SL952	VHF/UHF prescaler preamplifier	10, 87
SL955	VHF/UHF general purpose preamplifier	8, 89
SL1430	IF filter preamplifier	8, 91
SL1431	IF filter preamplifier with tuner AGC	8, 95
SL1432	IF filter preamplifier with tuner AGC	8, 95
SL1440	Parallel sound IF system	9, 99
SP4020	÷64 high speed divider	10, 102
SP4021	÷64 high speed divider	10, 102
SP4040	÷256 high speed divider	11, 103
SP4041	÷256 high speed divider	11, 103
SP4531	÷64 high speed divider	11, 107
SP4541	÷256 high speed divider	11, 111
SP4545	÷256/÷64 high speed divider	11, 113
SP4550	÷256 high speed divider	11, 115
SP4551	÷256 high speed divider	11, 115
SW153	SAW IF filter for UK PAL standard	8, 119
SW172	SAW IF filter for European PAL standard	9, 119
SW173	SAW IF filter for European PAL standard	8, 119
SW174	SAW IF filter for European PAL standard	8, 119
SW180	Parallel sound IF filter for European PAL standard	9
SW185	Parallel sound IF filter for European PAL standard	9, 129
SW203	SAW IF filter for American NTSC standard	9, 119

Selection guide

This is a selection guide by application to device type. It contains references to some devices (indicated in light type thus: SW180) not otherwise referred to in this databook. Full details of such devices can be obtained from Plessey Semiconductors Ltd., Customers Services, Crowdy's Hill Estate, Kembrey Street, Swindon, SN2 6BA, Wiltshire.

Devices marked thus:  form a family of integrated circuits for use in Multistandard PLL Frequency synthesis systems for TV. Devices marked thus: * are in the development stage.

INTEGRATED CIRCUITS FOR TELEVISION

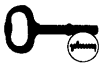
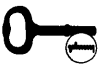
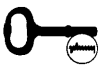
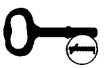
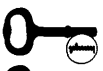
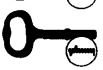
PREAMPLIFIER	**SL955**	General purpose 22dB amplifier for use at frequencies up to 1GHz
TUNING SELECTORS	**ML231B**	6-channel touch switch, with facility to select one input at switch-on
	ML232B	Similar to ML231B but with stepping facility
	ML238B	Similar to ML232B, but with 8 channels and mute
	ML239B	Similar to ML238B, but with negative input select
	ML237B	Similar to ML239B, but with only 6 channels
IF FILTER PREAMPLFIERS	**SL1430**	Ultra linear fixed gain preamplifier with differential output optimised for driving surface acoustic wave filters
	SL1431	Similar to SL1430 but with an internally derived NPN tuner AGC signal output
	SL1432	AS SL1431 but for PNP tuners
SURFACE ACOUSTIC WAVE, IF FILTERS	**SW153**	Complete TV IF filter with the frequency pass-band and phase response tailored for UK PAL colour television system I with a vision carrier frequency of 39.5 MHz
	SW173	As SW153 but for the European PAL standard, systems B and G with a vision carrier of 38.9MHz
	SW174	As SW173 but with higher performance and optimised for stereo sound

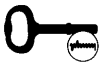
	SW172	Similar to SW174 but with a lower sound carrier for semi-parallel sound systems
	SW180	Similar to SW172 but with separate outputs for sound and vision signal processing
	SW185	As SW180 but with a vision carrier content in the sound output channel
	SW203	IF filter for the North American NTSC standard, systems M and N with a vision carrier frequency of 45.75 MHz
	SW250	IF filter for the French SECAM standard systems L and L' with a vision carrier frequency of 32.7 MHz
	SW260	IF filter for the Eastern European SECAM standard system D with a vision carrier frequency of 38 MHz
	SW453	IF filter for the South African PAL standard system I with vision carrier frequency of 38.9 MHz
VISION IF CIRCUITS	**TBA440N**	IF amplifier, synchronous detector and AGC system for NPN tuners
	TBA440P	As TBA440N for PNP tuners
	TDA440	High performance version of the TBA440P
	TDA2541	Similar to TDA440 but with AFC system
	TDA2540	As TDA2541 but for NPN tuners
	* **SL1440**	Parallel sound system with separate detectors for vision and sound carriers
SOUND IF CIRCUITS	**TBA120S**	Limiting IF amplifier with product detector for intercarrier FM sound and DC volume control
	TBA120U	Similar to TBA120S but with additional audio output before the volume control stage
	TBA120T	As TBA120U but designed for use with ceramic resonators for input and demodulator
	TBA750B	Similar to TBA120S but with separate audio preamplifier

COLOUR DECODERS	**TBA560C**	Luminance and chrominance control amplifiers with burst gating and colour killer facilities
	TDA2560	Similar to the TBA560C but with minimised external adjustments
	TBA540	Colour reference combination including colour subcarrier oscillator, ident, and ACC functions
	TCA800	Chroma demodulator, PAL switch, and matrix circuit providing clamped RGB outputs for single transistor drive
	TDA2522	Similar to TBA540 and TCA800 combination but providing colour difference outputs
	TDA2523	As TDA2522 but phase inverted to provide drive for transistor output stages
	TBA530	Used with TDA2522 to provide RGB outputs
	TDA2530	Similar to TBA530 but with clamped outputs
	TDA2532	As TDA2530 but with an extra data blanking input for use with on-screen displays, 'teletext' etc.
	TDA1365	Complete decoder, combines functions of TDA2522, TDA2560, and TDA2532
TIMEBASE CIRCUITS	**TBA920**	Sync separator and PLL horizontal oscillator
	TBA920S	As TBA920 but with lower phase error
	TBA950:2X	Similar to TBA920S but with vertical sync output
	TDA2590	Similar to TBA950:2X but providing 'sandcastle' blanking pulse output for use with TDA2530
	TDA2591	As TDA2590 but with modified timing and higher output current
	TDA2593	As TDA2591 but with modified sandcastle for use with TDA2532
	TDA9503	Similar to TDA2593 but for transistor drive only
DISPLAY DRIVERS	**CT2200**	Dual 7 segment display driver. 5-bit binary input, 1 to 32 display output
	ML2040	On-screen display for programme number, channel number, channel name, time and day. Control via "keybus"

INTEGRATED CIRCUITS FOR TV FREQUENCY SYNTHESIS

PRESCALER PREAMPLIFIER	**SL952**	VHF/UHF preamplifier to drive low sensitivity prescalers directly from the tuner's oscillator

PRESCALERS		**SP4020**	÷64 high speed divider with VHF and UHF inputs, suitable for frequencies up to 950MHz
		SP4021	As SP4020 but with a single input
		SP4040	Similar to SP4020 but ÷256
		SP4041	Similar to SP4021 but ÷256
		CT1010	÷64 high speed divider optimised for use with CT1011
		SP4551	High sensitivity 1GHz 5volt ÷256 divider with ECL type complementary outputs
		SP4550	As SP4551 but with a single output
		SP4531	Similar to SP4551 but ÷64
		SP4541	Similar to SP4551 but with a single TTL type output
		SP4545	Similar to SP4551 but switchable ratios ÷64 and ÷256
		**CT2010**	High sensitivity 1GHz 2 modulus ÷380/400 divider with low level output for "key system"
SYNTHESISER CIRCUITS		CT1011	÷15/16, Xtal oscillator, ÷4 and phase frequency comparator
		CT1133	Programmable divider, fine tune logic, and ROM for 100 TV channels
		**CT2012**	Basic PLL synthesiser including programmable divider, fine tune logic, Xtal oscillator, ÷1600 and phase frequency comparator
CONTROL CIRCUITS		CT1134	Control logic for 100 TV channels for use with CT1133
		CT2014	Multistandard control circuit for use with CT2012 providing 32 programmes, 400 channels, 4 standards, and fine tuning. Output via "keybus"
		CT2015	Similar to CT2014 but with channel sweep facility and remotely programmable
		CT1650	Microprocessor control circuit for use with CT2012 providing 32 programmes, 100 channels, single standard, fine tuning and channel sweep facility
KEYS ROMs		CT2030	ROM for up to 100 channels with frequency and name information for the European PAL standard. Accessed via "keybus" and with interface logic for a non-volatile programme memory
		CT2031	As CT2030 but for the French standard
		CT2032	As CT2030 but for the North American standard

		CT2033	As CT2030 but for the British Isles standard
INTERFACE CIRCUITS		CT1117	Active varicap line filter, band switch, and AV logic combination for use with CT1133
		**CT2017**	Tuner interface, active varicap line filter, station detector, AFC control, and power on detect

INTEGRATED CIRCUITS FOR REMOTE CONTROL

TRANSMITTERS		**SL490**	32 code PPM remote control transmitter with carrier oscillator. Possible transmission media include infra-red, ultrasonic, radio, and line
		SL491	As SL490 but optimised for non-carrier and multiple operation with burst mode
	* 	ML1900	56 code PPM remote control transmitter with power saving burst mode
RECEIVERS		**SL480**	Infra-red detector preamplifier with direct drive for ML series of receiver/decoders
		ML920	TV remote control receiver/decoder for use with SL490 or SL491. Providing 3 analogue outputs, 20 latched programmes, mute, etc.
		ML922	As ML920 but with 10 latched programmes
		ML923	Similar to ML920 but with a single analogue output and 16 latched programmes
	* 	ML1911	Multifunction remote control receiver decoder for use with ML1900. Providing 288 commands via "key-bus" including 6 analogues, and 32 programmes
	* 	ML1910	As ML1911 but with 55 code local control input
		ML928	Receiver/decoder for use with SL490 or SL491. Decodes the first 16 codes as 4 latched outputs
		ML929	As ML928 but operates from second set of 16 codes
		ML926	Similar to ML928 but decodes the first 15 codes as 4 momentary outputs
		ML927	As ML926 but operates from second set of 15 codes
		ML924	Receiver/decoder for use with SL490 or SL491. Decodes 32 codes to 5 bit parallel output and interrupt suitable for use with a microprocessor

	ML925	Multifunction receiver/decoder for use with SL490 or SL491. Provides control of traction motor, auxiliary motor, steering and other functions for toys and models

INTERFACE CIRCUITS

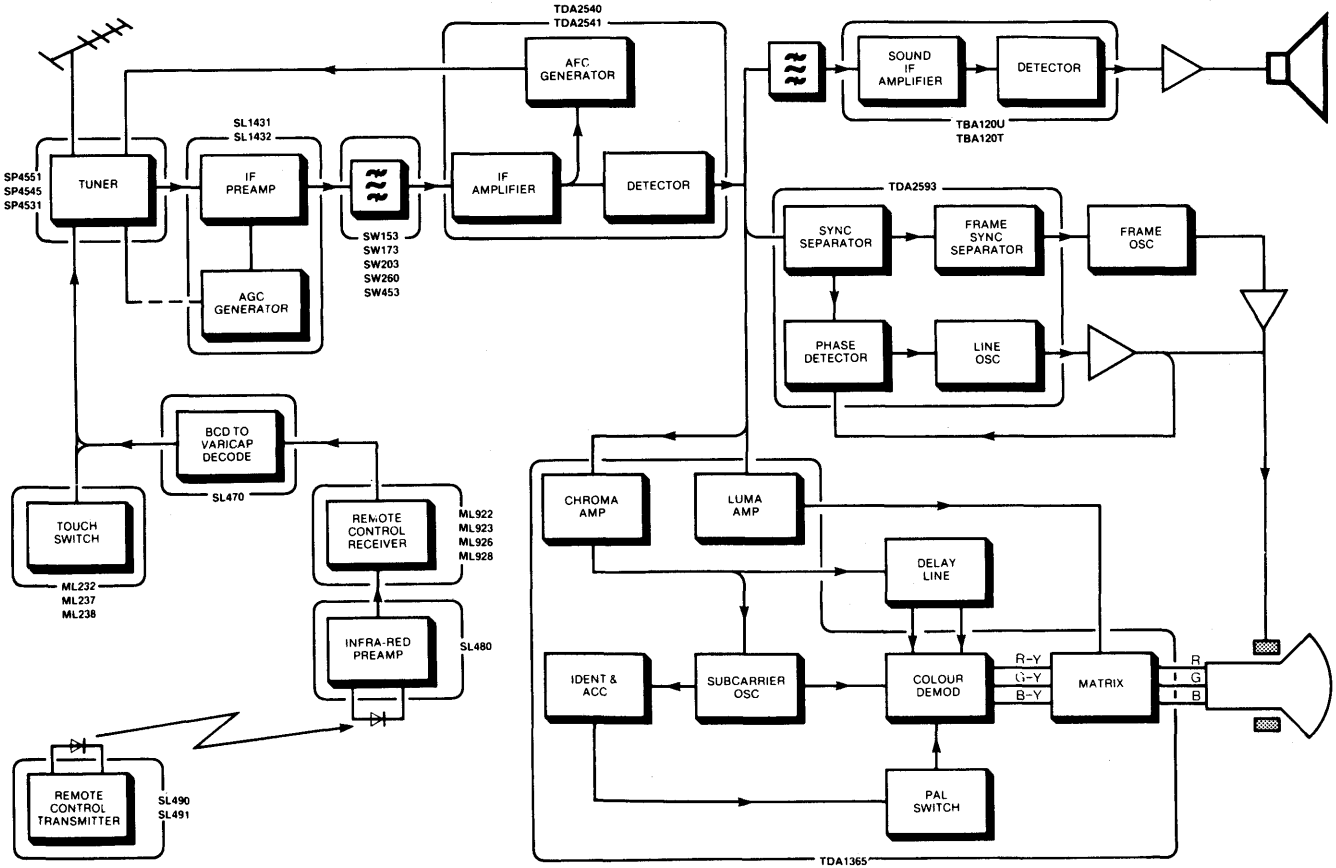
*	ML2001	Teletext/Viewdata control interface to "keybus"
	SL470	BCD to 1 out of 10 decoder/varicap driver

MAINTENANCE

These devices are for maintenance purposes only and are not recommended for new designs:

SW150	**SL439**	**SL901**	**SL917**	**SW400**
ML236	**SW170**	**TAA661**	**TBA550**	

INTEGRATED CIRCUITS FOR TV (PREFERRED SOLUTION)



Data sheet construction

The information in each data sheet in this data book is generally presented in the following order:

1. **Device description,** including one or more of the following: Features, Applications and Quick Reference Data.

2. **A pin connection diagram,** including a code reference to the preferred package outline shown at the end of the technical data. This code corresponds to the normal Pro-Electron package code with the addition of a number indicating the lead count, normally viewed from the top unless otherwise stated.

3. **A block diagram** of the integrated circuit.

4. **Absolute maximum ratings,** these are limiting values in accordance with the Absolute Maximum System IEC134, above which operating life may be curtailed or satisfactory performance impaired.

5. **Electrical characteristics**

6. **Operating notes**

7. **Typical application information**

Ordering information

U.K. ORDERS

Orders for quantities up to 99 received by Plessey Semiconductors Ltd. at Swindon will be referred automatically to our U.K. distributors; quantities of 1000 and over must be ordered from Plessey Semiconductors Ltd. direct, at the following address:

Plessey Semiconductors Ltd.,
Crowdy's Hill Estate,
Kembrey Street,
Swindon,
Wiltshire SN2 6BA
Tel: (0793) 694994
Telex: 449637

OVERSEAS ORDERS

Products contained in this databook can be ordered from your listed Plessey Office, Agent or Distributor.

PLESSEY SEMICONDUCTORS IC TYPE NUMBERING

Plessey Semiconductors Ltd. integrated circuits are allocated type numbers which must be used when ordering. The Pro-Electron code is used to identify package outlines.

CM – Multilead TO
DG – Ceramic Dual In-Line
DP – Plastic Dual In-Line
QP – Plastic Quad In-Line

This package code is for reference purposes only and need only be used when ordering where a device is offered in more than one package style. The package code does not appear on the device itself.

Quality data

DELIVERED PRODUCT QUALITY

It is our policy to deliver a reliable quality product and to achieve this end all devices undergo 100% electrical testing of every relevant AC and DC parameter prior to shipment. The devices are tested under conditions of level and frequency closely simulating those of the typical application. Fully automatic Teradyne integrated circuit test machines, acknowledged to be among the best computer controlled test machines available, are employed.

Each and every stage of processing, assembly and testing is carefully audited by Plessey Semiconductors' independent Quality Assurance department.

Therefore we are able to guarantee the following Acceptable Quality Level (A.Q.L.) on all deliveries.

MECHANICAL

Defects of a mechanical nature including coding not being legible, deformed leads, dimensional tolerances being exceeded, wrong identification of pin 1 and pins not being solderable.

0.65 %AQL, I.L. II

ELECTRICAL

Defects of an electrical nature including device parameters being outside the acceptance specification limits, or those only stated as typical being grossly in error.

0.4 %AQL, I.L. II

The average delivered product quality is considerably better than this, the population of imperfect devices being much smaller than that indicated by the AQL values which reflect the sampling plans used by QA in the Test and Code departments.

RANDOM SAMPLE TESTING

Sample sizes and accept/reject criteria are drawn from the following table.

Random sampling test plan for normal inspection. Similar to BS6001 (MIL-Std. 105D), inspection level II

Lot Size	Sample Size	AQL VALUE%											
		0.065	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5	
		Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	
2 to 8	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	
9 to 15	3										0 1	↑ ↓	
16 to 25	5									0 1	↑		
26 to 50	8						↓	↓	0 1	↑ ↓	↓	1 2	
51 to 90	13							0 1	↑		1 2	2 3	
91 to 150	20					↓	0 1	↑	↓	1 2	2 3	3 4	
151 to 280	32				↓	0 1	↑	↓	1 2	2 3	3 4	5 6	
281 to 500	50				0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	
501 to 1200	80		↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	
1201 to 3200	125	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	
3200 to 10000	200	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	
10001 to 35000	315	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑ ↑	
35001 – 150000	500	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑ ↑		
150001 – 500000	800	1 2	2 3	3 4	4 6	7 8	10 11	14 15	21 22	↑ ↑			
500000 and more	1250	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑ ↑				

↑ **Use first sampling plan shown above arrow**

↓ **Use first sampling plan shown below arrow**

Ac = Acceptance number = the number of defective devices in the sample at or below which the lot is acceptable.
Re = Rejection number = the number of defective devices in the sample at or above which the lot is rejected.

Soldering information

All devices must be protected against overheating during the soldering process. If the following maximum conditions cannot be satisfied some form of thermal shunt or, in the case of flow soldering, after bath cooling stage must be employed. At no time should the device's case temperature be allowed to exceed the maximum storage temperature.

MAXIMUM CONDITIONS

a) Soldering iron method

Devices may be soldered directly into a circuit board as long as the iron tip is applied at least 1.5mm from the device case. A maximum tip temperature of 245°C may be applied for up to 10 seconds or 350°C for up to 5 seconds.

b) Flow soldering method

For devices mounted with their seating planes flush with punched-through hole printed circuit board, or spaced 1mm from plated-through circuit board a maximum solder temperature of 245°C can be employed for up to 4 seconds or 260°C for up to 3 seconds.

Technical Data

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ADVANCE INFORMATION

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CT2010

1 GHz ÷ 380/400 PRESCALER

The CT2010 is a 380/400 two modulus divider which will operate at frequencies between 80 MHz and 1 GHz. The device is the prescaler used in the Plessey Key Frequency Synthesis Tuning System.

The input is terminated by a nominal 50 ohms and should be AC coupled to the signal source. The reference pin should be AC decoupled. The decoupling should be effective over the full operating frequency range.

The divider contains a fixed divide by 20 followed by a divide by 19/20. The divide by 19/20 divides by 20 when no control pulses are applied to the control input. The divide by 19/20 will divide by 19 once for every positive going edge applied to the control pin. The control input edge is latched and synchronised so that the following output cycle, commencing with a negative edge, is produced by 380 input cycles to the whole divider stage, rather than 400. This means that the device is highly tolerant of delay in the control loop and distortion of the control waveform.

To ensure that there is an output cycle produced by 380 input cycles for every control pulse, the rate of control pulses should not exceed half the output frequency. (See timing diagrams.)

The output source impedance is nominally 100 ohms. The output swing is nominally 300 mV and swings down from the positive supply.

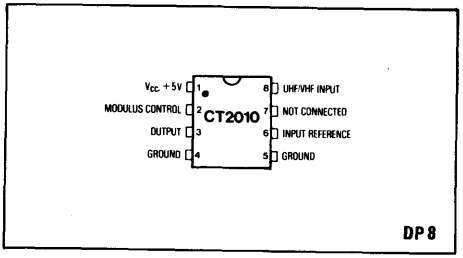

Fig.1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7V
UHF input voltage	2.5V p-p
Storage temperature	-55°C to +125°C
Operating ambient temperature	-10°C to +65°C

FEATURES

- On-chip Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Low Output Radiation
- Single ECL Output
- 5V Logic Level Control Input
- Control Independent of Distortion and Delay

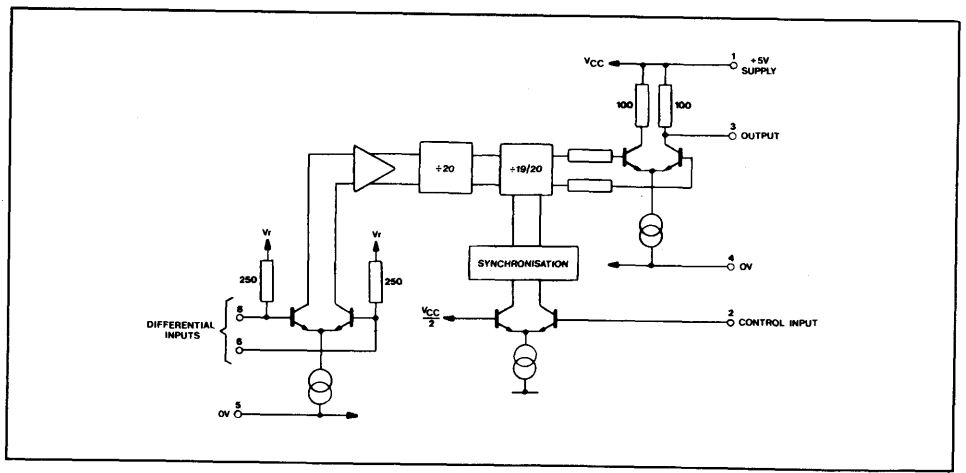

Fig.2 CT2010 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Test circuit: Fig.3
V_{cc} = 5V, T_{amb} = 25°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range	1	4.5		5.5	V	
Supply current	1		90	110	mA	
Input voltage, 80MHz	8, 6	17.5		200	mV	rms, sine wave 50Ω
V_{IN} 300MHz	8, 6	17.5		200	mV	rms, sine wave 50Ω
500MHz	8, 6	17.5		200	mV	rms, sine wave 50Ω
700MHz	8, 6	17.5		200	mV	rms, sine wave 50Ω
1000MHz	8, 6	17.5		200	mV	rms, sine wave 50Ω
Output voltage swing	3	240	300		mV	p-p, no load
Output impedance	3		100		Ω	
Control input, high	2	$2/3V_{cc}$				
	2			50	μA	
low	2			$1/3V_{cc}$		
	2	-10			μA	
pulse width	2	0.2	3		μS	

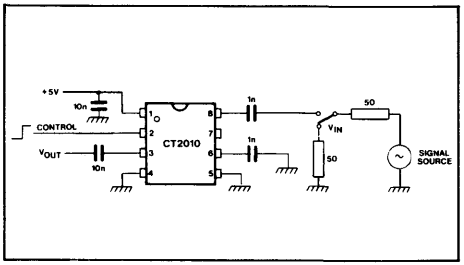

Fig.3 Test configuration

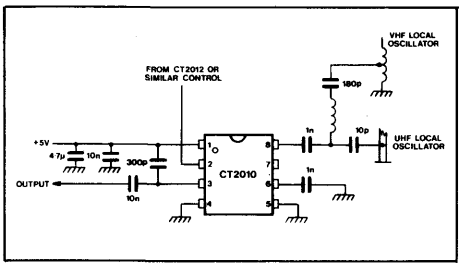

Fig.4 Typical application with combined input

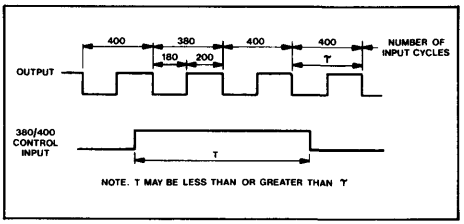

Fig.5 Timing diagram

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CT2012

PLL SYNTHESISER FOR TV

The CT2012 forms the heart of the Plessey Key Frequency Synthesis Tuning System by taking data from the system control and data highway (the Keybus) when TUNE or FINE TUNE code is recognised and then using this data to control the frequency of the local oscillator in a television tuner with a phase locked loop (PLL).

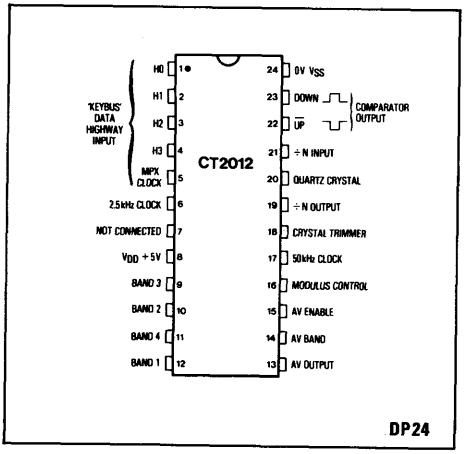


Fig.1 Pin connections

FEATURES

- High Sensitivity Divider Input
- Improved Control of Two-Modulus Divider
- Fully Keybus Controlled
- On-chip Frequency Standard and Comparator
- Four Band Selection Outputs

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	+7V
Pin Voltage, pins 9—13	+14V
Voltage, all other pins	+7V
Operating temperature range	-10°C to +65°C
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = +5V
Test circuit: Fig.3

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range	8	4.5		5.5	V	
Supply current	8		22	45	mA	Outputs unloaded
Keybus inputs, high	1—5	V_{DD} -1			V	Leakage 10μA max.(Pin 5 only)
low	1—5			0.8	V	
Internal pullup resistor	1—4	2	4	6	kΩ	
÷N input, peak-peak swing	21	200			mV	Sine wave via external capacitor
Internal capacitance	21			10	pF	
External frequency standard input, pin 20 not connected high	18	V_{DD} -1			V	100μA max. sinking
low	18			0.8	V	100μA max. sourcing
Quartz crystal standard	18, 20		4		MHz	20pF parallel resonance
AV Band and enable inputs	14, 15	V_{DD} -1			V	Leakage 10μA max.
	14, 15			0.8	V	
Band and AV outputs, unselected	9—13			13.2	V	Free drain, leakage 10μA max.
selected	9—13			5	V	1mA sinking
÷N output, high	19			7	V	Free drain, leakage 10μA max.
low	19			0.4	V	0.3mA sinking

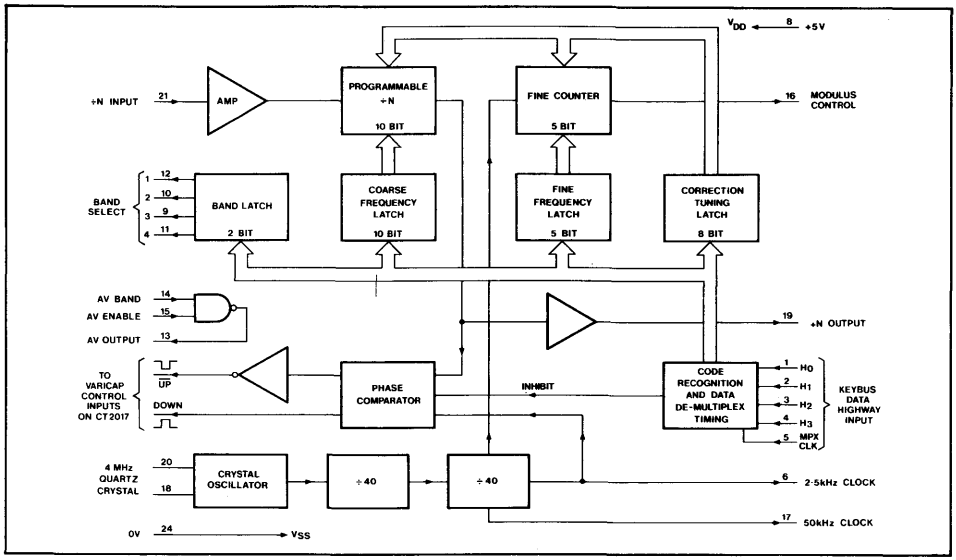


Fig.2 CT2012 block diagram

Apart from the CT2012 and the tuner, the PLL needs two other integrated circuits: a ÷380/400 PRESCALER (the CT2010) and the synthesiser tuning interface (the CT2017), which includes a charge pump, an active filter and an output stage to drive the varicap line which controls the local oscillator in the tuner.

In a typical system re-tuning of the television receiver will come from a control circuit (such as the CT2014) following some input from the viewer. This input will be new channel, fine tuning information or an instruction to access a word of non-volatile memory. In every case, the control circuit will send the required channel and fine tuning information to the CT2012.

The FINE TUNE code is used to directly transfer the FINE TUNE number from the control circuit to the synthesiser and is separate from TUNE to reduce the highway use and the time delay during manual and automatic adjustment tuning.

The CT2012 contains six main parts:

(a) A section to recognise the TUNE code (hexadecimal 1D) or FINE TUNE code (hex. 1E) on the Keybus and then to latch all of the relevant tuning information.

(b) A 10 bit programmable divider with an amplifier on its clock input to allow use of a small swing on the output of the PRESCALER and hence to reduce radiation.

(c) A fine tuning system which generates the correct pulses to control the modulus of the prescaler and so give a small shift in synthesised frequency.

(d) A crystal oscillator circuit (for 4MHz crystal) and fixed ÷1600 divider to give 2.5kHz comparison frequency and fine tuning timing.

(e) A phase and frequency comparator driven by the programmable divider and the fixed divider.

(f) Logic for band decoding and for video time-constant switching for audio visual (AV) mode logic.

The Keybus highway is used to carry both instructions and data around the Key System. To separate these two functions the codes are transmitted when the Multiplex Clock is low and the data when it is high; all zeroes or all ones are inserted to fill the gaps between adjacent code or data words to avoid spurious instructions. In order to improve the system's immunity to noise on the highway the Multiplex Clock may be stopped between operations so that noise is not clocked into any circuit, and so should have no effect, and ideally the highway and Multiplex Clock lines will be stopped in their lower impedance state to reduce noise amplitudes.

It is expected that all devices driving the highway will have Open Drain outputs, for which pull-up resistors (nominal 4kΩ) are included in the CT2012.

To safely detect control codes edge sensitive latches are clocked on the rising ('0' to '1') edges of the Multiplex Clock and have their inputs driven by gates looking for a TUNE code (0001 followed by 1101) or a FINE TUNE (0001 followed by 1110).

Time	State				Remarks
	H3	H2	H1	H0	
C1	0	0	0	1	Control code
C2	1	1	0	1	
D1					Not used by Synthesiser
D2					
D3					
D4	B1	B0	Q9	Q8	Band (B), Frequency (Q) and Fine Frequency (P) from Key.
D5	Q7	Q6	Q5	Q4	
D6	Q3	Q2	Q1	Q0	
D7	0	0	0	P4	
D8	P3	P2	P1	P0	

Table 1 Tuning sequence on Keybus

Time	State				Remarks
	H3	H2	H1	H0	
C1	0	0	0	1	Control code
C2	1	1	1	0	
D1	Q_{C2}	Q_{C1}	Q_{C0}	P_{C4}	Correction tuning
D2	P_{C3}	P_{C2}	P_{C1}	P_{C0}	

Table 2 Correction tuning sequence on Keybus

Signal	Pin	High (source current) V_{DD} – 0.5 V min	Low (sink current) 0.4 V max
2.5kHz Clock	6	0.5mA	2.0mA
$\overline{UP}$ DOWN 50kHz Clock	22 23 17	0.1mA	0.8mA
Modulus Control	16	0.1mA	0.3mA

Table 3 Logic output currents

Pin No.	Name	Function	
8 24	V_{DD} V_{SS}	+5V 0V } Power supply	
1 2 3 4	H0 H1 H2 H3	Four line highway, H0 is LSB. Inputs, 0V and 5V logic levels nominal. 4K ±50% pull-up resistors (to V_{DD}) in device.	KEYBUS
5	MULTIPLEX CLOCK	Highway timing input, 0V and 5V nominal logic levels.	
6	2.5kHz CLOCK	2.5kHz output from crystal via reference divider. May be used to give Multiplex Clock.	Outputs with 0V to 5V nominal swing
17	50kHz CLOCK	50kHz output from crystal via reference divider. Use when setting crystal trimmer.	
22 23	$\overline{UP}$ DOWN	Increase frequency when low Decrease frequency when high } Comparator outputs to charge pump in Tuning Interface IC	
16	MODULUS CONTROL	Controls PRESCALER division ratio by pulsing high up to 38 times each comparison cycle.	
20	QUARTZ CRYSTAL	One crystal pin and the fixed capacitor.	
18	QUARTZ CRYSTAL TRIMMER	Second crystal pin and trimmer capacitor.	
21	÷N INPUT	Low level input clock to Programmable Divider. Should be AC coupled.	
12 9 11 10 13	BAND 1 BAND 3 BAND 4 BAND 2 AV OUTPUT	Band output selected by code 00 Band output selected by code 01 Band output selected by code 10 Band output selected by code 11 Time constant switch, pulls low only if AV band selected and AV enable is high	Open drain outputs for external pull-up to +12V.
14	AV BAND	Input from band switch to allow AV mode to be selected.	
15	AV ENABLE	Selects shorter time constants for locking television receiver to video tape recorder or equivalent. Will be driven by diode decoder from Programme Number lines. High for AV mode, only operative when AV band is selected.	
19	÷N OUTPUT	Output of programmable divider provided for test purposes only.	

TUNING RANGE

Combining the Fine Offset range, 0 to 19 steps of 50kHz with the Programmable Divider range, 80 to 1023 steps of 1MHz, allows tuning of the local oscillator for all television broadcast channels in bands I, III, IV, V, to within 25kHz. In practice almost all television channels are integer multiples of 50kHz and so may be received EXACTLY (apart from any slight crystal or IF error).

The correction tuning system gives a range of -3.95 to +4.00MHz in 50kHz steps around the nominal frequency.

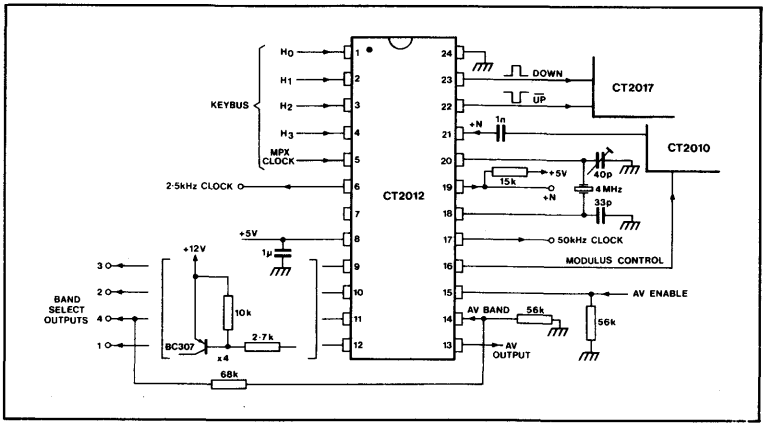


Fig.3 CT2012 test and application circuit

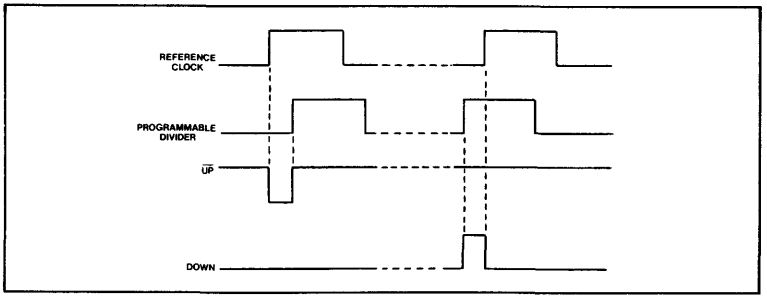
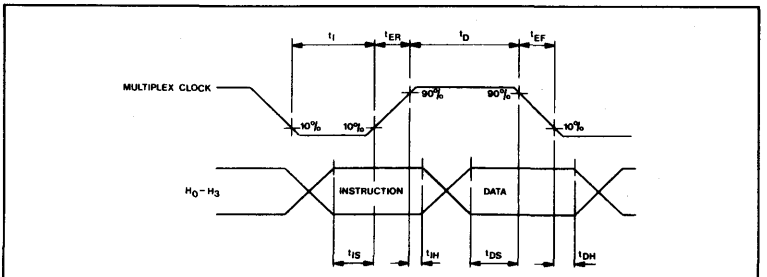


Fig.4 Phase comparator timing



Multiplex Clock:

Instruction or data time (t_I or t_D)	:	1μs minimum
Rising or falling edge time (t_{ER} or t_{EF})	:	200ns maximum
Data or instruction to clock set-up time (t_{DS} or t_{IS})	:	400ns minimum
Clock to data or instruction hold time (t_{DH} or t_{IH})	:	100ns minimum
Operating frequency range of Multiplex Clock	:	DC - 500kHz
$\div N_{IN}$ frequency	:	2.8MHz maximum
	:	100kHz minimum

Fig.5 Dynamic characteristics

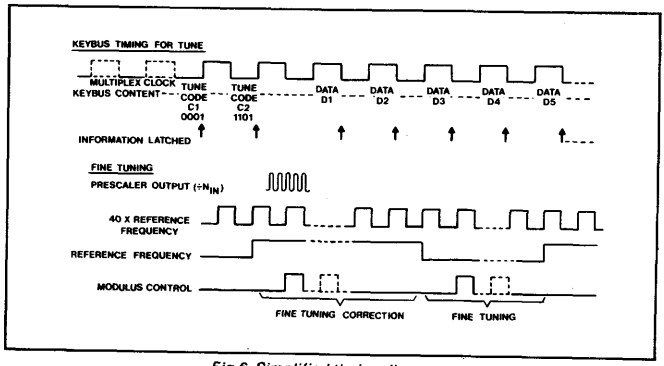


Fig.6 Simplified timing diagrams

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CT2017

SYNTHESISER TUNING INTERFACE

The CT2017 is designed for use in Frequency Synthesis Tuning Systems, in particular the Plessey Key System.

The device contains a charge pump with a high impedance voltage follower, a signal detect circuit, a digital AFC circuit and a power on low detect circuit.

FEATURES

- Low Varicap Driver
- Active Filter Charge Pump
- Logic Level Control
- Signal Quality Detector
- AFC Input Option
- Auto Up, Auto Down Logic Level Tuning Correction
- Power Low Detector

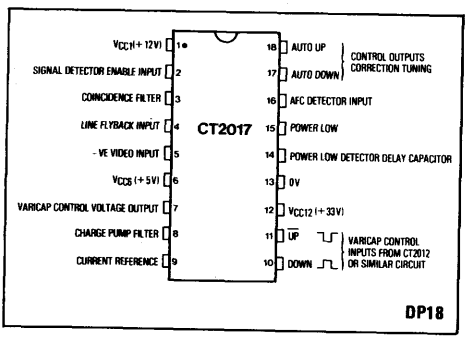


Fig.1 Pin connections

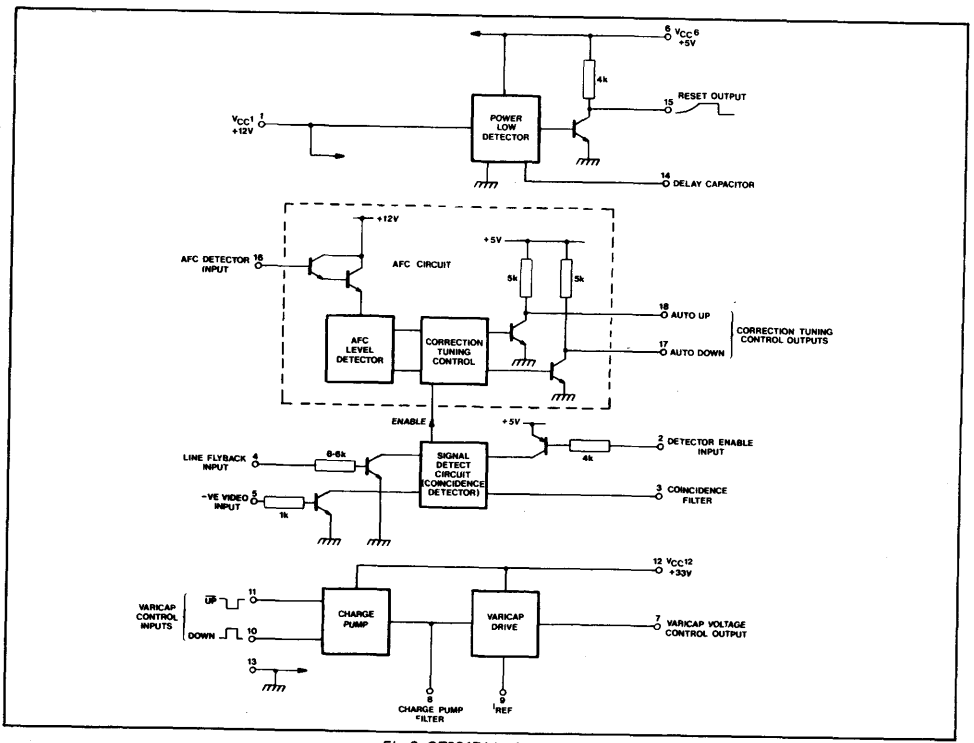


Fig.2 CT2017 block diagram

The charge pump is operated by two 5V logic inputs $\overline{UP}$ (active low) and DOWN (active high). These inputs turn on a charge current and discharge current respectively. The charge pump circuit and its voltage follower operate from the +33V supply rail. The combined charge pump, external filter and voltage follower may be used as the filter and varicap driver for synthesis tuning systems.

The signal detect circuit is used in tuning systems capable of automatically sweeping the received broadcast bands. The circuit examines the line synchronisation pulse and line flyback pulse for coincidence. When a regular supply of adequate coincident line synchronisation pulses occurs, the filter voltage falls. This indicates a received signal of a sufficient strength to produce a viewable picture.

When the signal detect filter voltage is higher than the signal detectors threshold the AUTO UP and AUTO DOWN outputs are clamped at Logic '0'. When the filter detect voltage is below the level detector's threshold the AUTO UP and AUTO DOWN outputs are enabled. The enabling of AUTO UP and AUTO DOWN may be used to indicate that a signal of adequate strength has been received and the sweep may be stopped.

Using appropriate external components, pin 5 may be used as a sync pulse separator, when fed with negative video or a positive line sync pulse input.

The signal strength recognised as good depends on the signal to noise ratio at the input to pin 5. This will depend on the type of sync separation used, whether noise gating is used and the noise figure of the signal processing circuits.

A digital AFC circuit, which comprises AFC level detector and correction tuning control, examines the AFC signal ('S' curve) produced by conventional television AFC circuits. The circuit produces an AUTO UP Logic '1' output when the AFC voltage is greater than the upper AFC threshold, and an AUTO DOWN Logic '1' output when the AFC voltage falls below the lower AFC threshold. Both outputs are Logic '0' when the AFC voltage is between the upper and lower thresholds.

CORRECTION TUNING

The AUTO UP and AUTO DOWN outputs may be used to adjust the correction tuning number of a synthesis tuning system and hence produce a digitally quantised AFC.

The power low detector circuit compares the +5V supply and the +12V supply against internal reference levels. When either supply falls below its relevant reference level the delay capacitor is discharged and the power low detector reset output is set to logic '1'. When the supplies exceed their relevant reference levels, the delay capacitor is charged to the threshold level, which turns on a transistor and the output is set to logic '0' after a delay.

The resulting output pulse may be used for setting the logic of the tuning synthesiser and for protecting the memory from corruption during power on and power off.

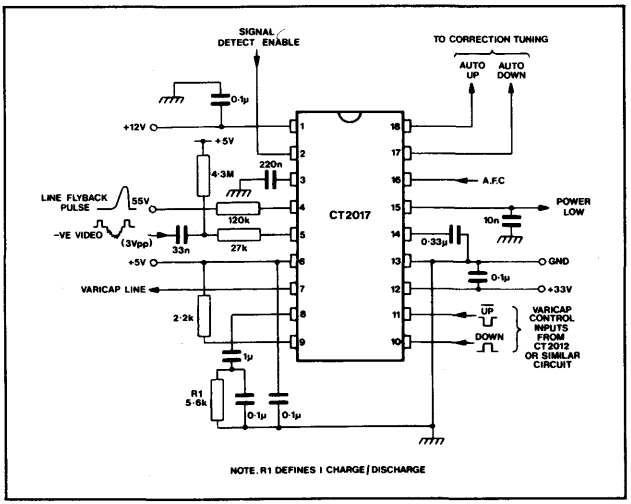
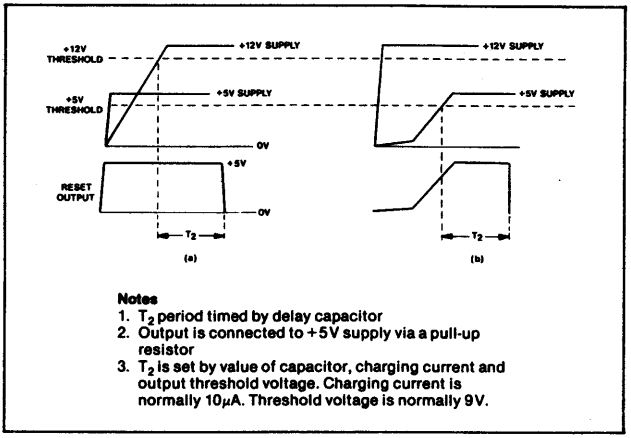


Fig.3 Test and application circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$, $V_{CC1} = +12V$, $V_{CC6} = +5V$, $V_{CC12} = +33V$
Test circuit: Fig.3

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range						
V_{CC1} (+12V)	1	10.8		13.2	V	
V_{CC6} (+5V)	6	4.5		5.5	V	
V_{CC12} (+33V)	12	31		36	V	
Supply current						
V_{CC1} (+12V)	1		8	12	mA	
V_{CC6} (+5V)	6		12	20	mA	$V_5 = 0V$, $V_{10} = 0V$, $V_{11} = 5V$
V_{CC12} (+33V)	12	3.3	4.5	5.5	mA	$I_9 = 2mA$, $V_{10} = 0V$, $V_{11} = +5V$
Varicap control						
Output range available	7	0.9		29.5	V	$I_9 = 2mA$ (R_9 2.2kΩ) $V_{CC}12 = 33.0V$
Output leakage current	7			40	nA	$V_{11} = +5V$, $V_{10} = 0V$
$\overline{UP}$ control input active	11			1	V	
$\overline{UP}$ control input inactive	11	3			V	
$\overline{UP}$ control input current	11			50	μA	$V_{11} = +5V$
DOWN control input active	10	3			V	
DOWN control input inactive	10			1	V	
DOWN control input current	10			50	μA	$V_{10} = +5V$
AFC control						
Detector high threshold	16	7.0	7.5	8.0	V	
Detector low threshold	16	4.1	4.5	4.9	V	
Detector window	16	2.8	3.0	3.2	V	
Input current	16			2.5	μA	$V_{16} = +12V$
Correction tuning outputs (AUTO UP, AUTO DOWN)						
Voltage high	17, 18	4.5			V	V_{17} high = DOWN, V_{18} high = UP Current source = 50μA
Voltage low	17, 18			0.5	V	Both low = inactive, current sink = 2mA
Line flyback threshold						
High	4	2			V	
Low	4			0.7	V	
Negative video input						
Threshold	5		0.7		V	
Sync pulse switching current	5			12	μA	
Leakage current	5			0.3	μA	$V_5 = -5V$
Coincidence detector						
Enable	2	4.5			V	
Inhibit	2			2	V	
Threshold	3		2.4		V	
Power on detector						
Output voltage	15	4.5			V	Current source = 50μA
Normal				0.5	V	Current sink = 2mA
Detector threshold						
V_{CC1} (+12V)	1	9.2	9.9	10.6	V	See Figs.4 and 5
V_{CC6} (+5V)	6	3.7	4	4.3	V	See Figs.4 and 5
Delay capacitor charging current	14		10		μA	
Delay threshold	14		9		V	



Notes

1. T_2 period timed by delay capacitor
2. Output is connected to +5V supply via a pull-up resistor
3. T_2 is set by value of capacitor, charging current and output threshold voltage. Charging current is normally 10μA. Threshold voltage is normally 9V.

Fig.4 Power low detector timing diagram (Power on)

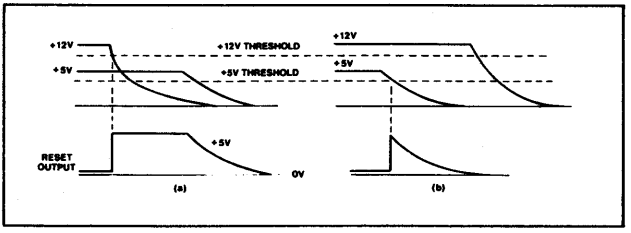


Fig.5 Power low detector timing diagram (Power off)

ABSOLUTE MAXIMUM RATINGS

+12V supply (V_{CC1})	+20V
+5V supply (V_{CC5})	+20V
+33V supply (V_{CC12})	+40V
Operating temperature range	-10°C to +65°C
Storage temperature range	-55°C to +125°C

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CT2200

5-BIT BINARY TO 13-SEGMENT DECODER/DRIVER

The CT2200 is an N-channel MOS integrated circuit, designed to directly drive two 7-segment LEDs to display the numbers 1 to 32, with leading zeros suppressed. The circuit is ideal for applications such as the programme number display of a television receiver. The display is controlled by a 5-bit binary input port, weighted so that the number shown (1-32) is one more than the binary input (0-31) to avoid programme 0. The 5 lines can come from a remote control receiver or from any other source of continuous 5-bit data.

Common anode LEDs can be driven directly with a current limiting resistor in series with each output (see Fig.5) or by using some other form of brightness control (see Fig.6). By driving each segment individually the interference problems associated with multiplexed displays are avoided.

A blanking input is provided so that the display can be turned off or can be made to flash with an external pulsed signal.

Only 13 lines are needed for two 7-segment displays because segment Tf is never lit for the numbers 1 to 32 and so does not need to be decoded and driven. Segment identification is shown in Fig.2.

The 13 outputs of the output encoder drive the gates of large output transistors to give two states: OFF and SINK CURRENT; as there can be up to 12 outputs on at once, each sinking 20mA, four 0V pins are provided to reliably carry this current. **ALL FOUR PINS (3, 7, 18, 22) MUST BE CONNECTED TO 0V.**

The number of segments required for each character is shown in Fig.3.

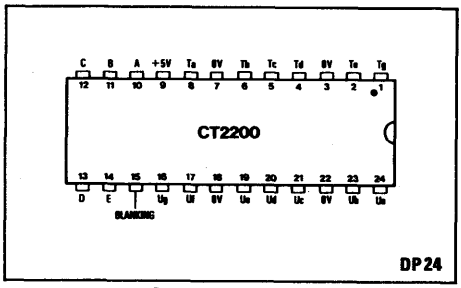

Fig.1 Pin connections

FEATURES

- Direct Segment Drive — Non-Multiplexed
- 5V Supply
- Blanking Input
- Leading Zero Suppressed
- Minimum Segment Pattern per Character
- 20mA Drive per Segment
- 5-Bit Binary Input

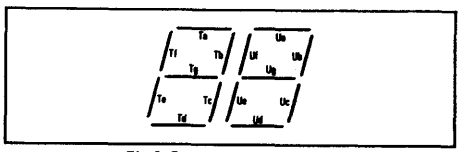

Fig.2 Segment identification

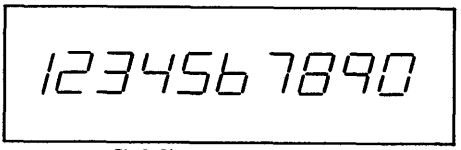

Fig.3 Character representation

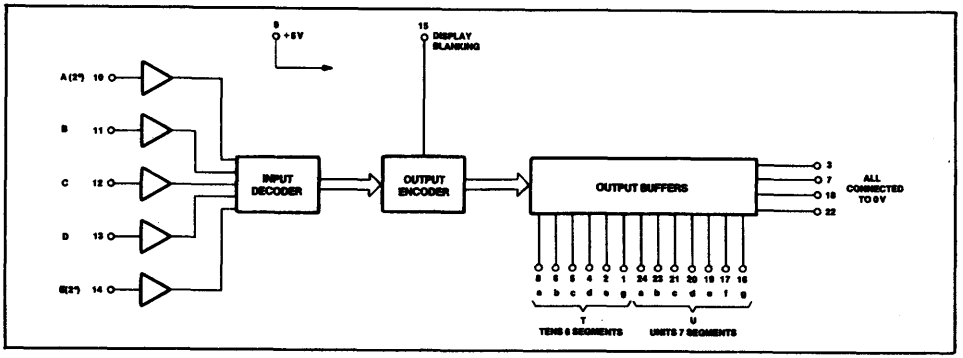

Fig.4 Block diagram

ELECTRICAL CHARACTERISTICS (see Fig.5)

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$, $V_{DD} = +5V$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range	9	4.5	5	5.5	V	
Supply current	9			5	mA	
Input voltage high	10-14	4			V	
Input voltage low	10-14			0.8	V	
Leakage current	10-14			10	μA	$V_{IN} = +5V$
Capacitance	10-14			10	pF	
Output voltage	1, 2, 4-6, 8, 16, 17, 19-21 23, 24			1	V	Sinking 20mA
Recommended series resistor (if used)			120		Ω	

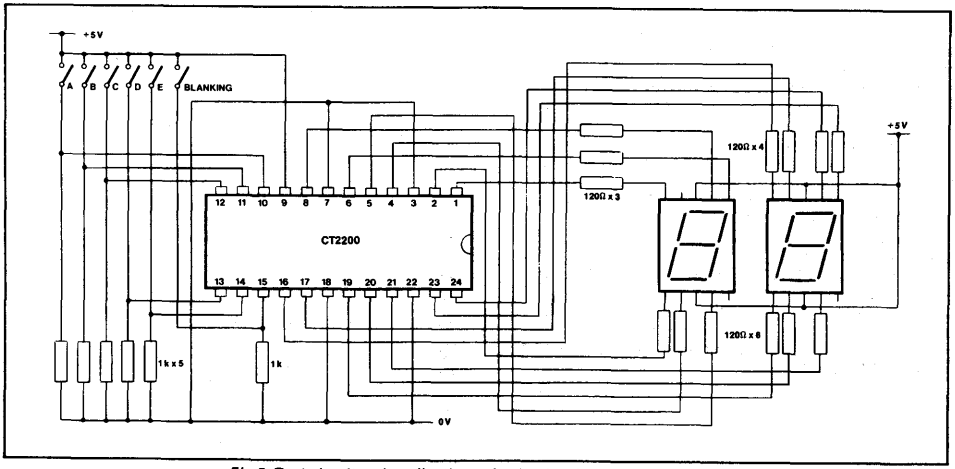

Fig.5 Test circuit and application using load resistors (see also Fig.6)

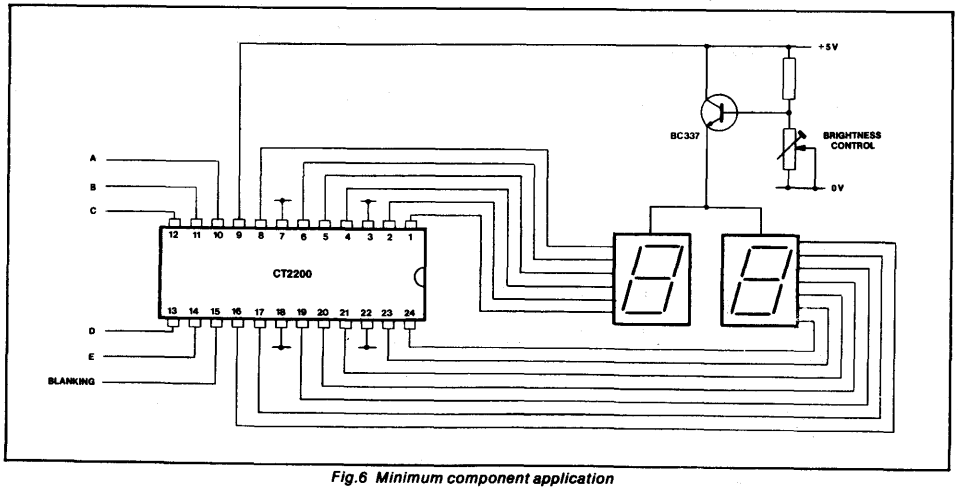

Fig.6 Minimum component application

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	+7V
Input or output voltage	+7V
Output current	30mA
Ambient operating temperature	-10°C to +65°C
Storage temperature	-55°C to +125°C

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ML231B

MOS TOUCH TUNER

The ML231B is a six-channel sense circuit designed specifically for touch tuning in colour and monochrome television receivers. Using low threshold P-MOS technology, the circuit can be driven directly from two-terminal touch plates — replacing conventional mechanical push-buttons for channel selection. Neons may be used to indicate the selected channel, while the latched output of the ML231B drives the varicap tuner via a bias selection network.

An additional output is provided which goes high with no channel selected and may be used externally to select channel 3 so as to prevent the existence of a null state.

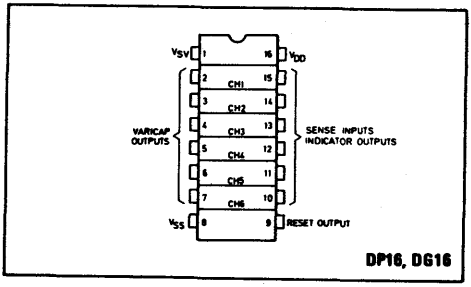


Fig. 1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	−10°C to +65°C
Storage temperature	−10°C to +85°C
Supply, Vss–VDD	36V
Varicap voltage Vsv w.r.t. Vss	+0.3V

FEATURES

- Six-channel Capability
- Direct Neon or LED Drive
- Low Impedance Drive to Varicap
- Uses 33V Varicap Supply
- Low Current Drain
- Reset O/P Prevents Null State

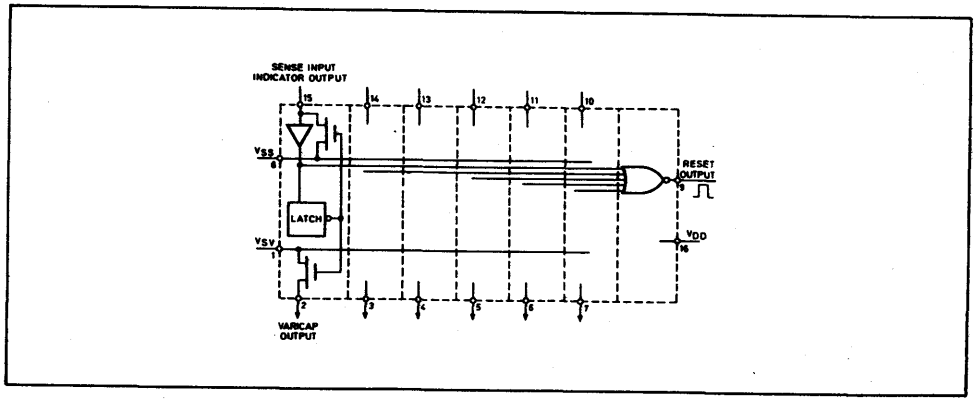


Fig. 2 Functional diagram (positive logic)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 0, V_{SS} = V_{SV} = 30V to 36V

Characteristic	Value			Units	Condition
	Min.	Typ.	Max.		
Input current			1	μA	V_{in} = 0V
Supply current	2	4	5.5	mA	
R_{ON} of varicap switch		50	100	Ω	Iout = 10mA
R_{ON} indicator switch		125	250	Ω	Iout = 4mA
Sense input threshold	0.4V_{SS}	0.5V_{SS}	0.6V_{SS}	V	
Reset O/P voltage high	V_{SS} −10			V	Iout = 0.5mA

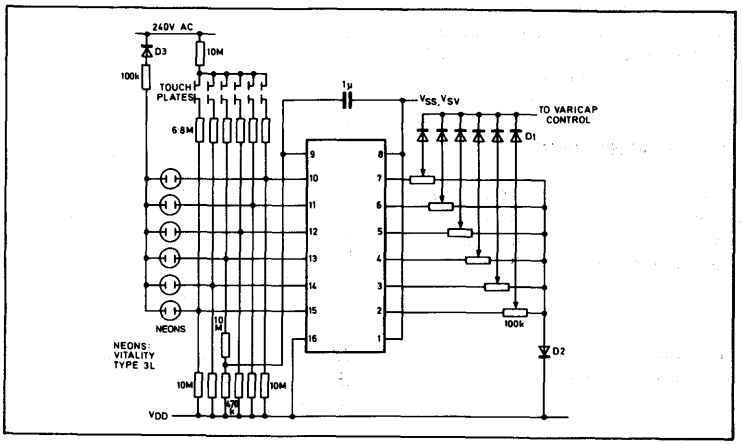


Fig. 3 Typical application circuit

Reset output = $\overline{CH1} \cdot \overline{CH2} \cdot \overline{CH4} \cdot \overline{CH5} \cdot \overline{CH6}$

= $\overline{1+2+3+4+5+6+3}$

PLESSEY
Semiconductors

ML232B

MOS TOUCH TUNER

The ML232B is a six-channel sense circuit designed specifically for touch tuning in colour and monochrome television receivers. Using low threshold P-MOS technology, the circuit can be driven directly from two-terminal touch plates — replacing conventional mechanical push-buttons for channel selection. Neons may be used to indicate the selected channel, while the latched output of the ML232B drives the varicap tuner via a bias selection network.

A stepping facility is included whereby the application of a suitable negative-going pulse to the step input pin, will cause the selected channel output to advance by one.

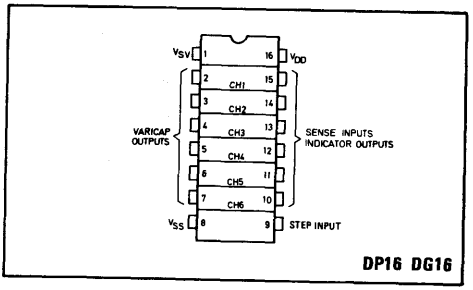


Fig. 1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	−10°C to +65°C
Storage temperature	−10°C to +85°C
Supply, V_{SS}–V_{DD}	36V
Varicap voltage V_{SV} w.r.t. V_{SS}	+0.3V

FEATURES

- Six-channel Capability
- Direct Neon or LED Drive
- Low Impedance Drive to Varicap
- Uses 33V Varicap Supply
- Low Current Drain
- Remote Control Stepping Facility

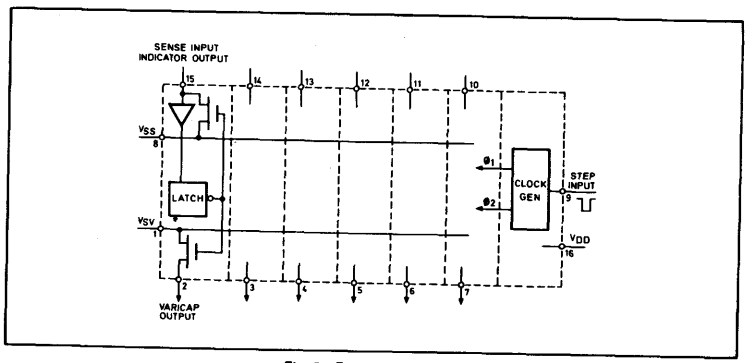


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

$T_{amb.}$ = +25°C, V_{DD} = 0, V_{SS} = V_{SV} = 30V to 36V

Characteristic	Value			Units	Condition
	Min.	Typ.	Max.		
Input current			1	μA	V_{in} = 0V
Supply current	2	4	5.5	mA	
R_{ON} of varicap switch		50	100	Ω	Iout = 10mA
R_{ON} of indicator switch		125	250	Ω	Iout = 4mA
Sense input threshold	0.4V_{SS}	0.5V_{SS}	0.6V_{SS}	V	
Step pulse level	0		V_{SS} −29	V	
Step pulse width	0.1		1	ms	T_{amb} = 0°C to +65°C

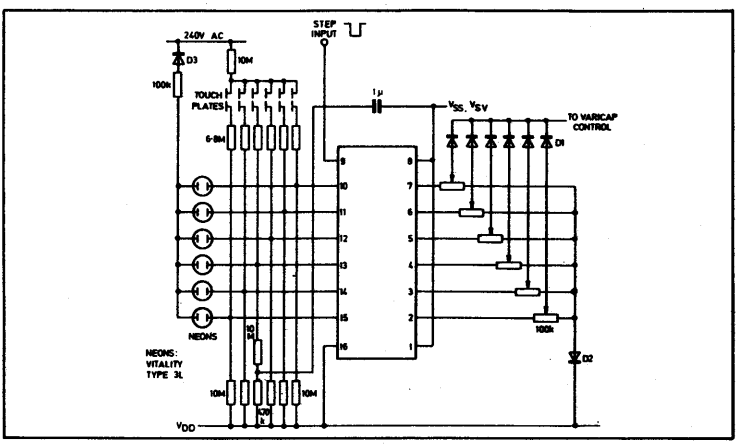


Fig. 3 Typical application circuit

PLESSEY
Semiconductors

ML237B

6-CHANNEL TOUCH CONTROL INTERFACE

The ML237B is a six-channel sense circuit designed specifically for touch tuning in colour and monochrome television receivers. Using low threshold P-MOS technology, the circuit can be driven directly from two-terminal touch plates — replacing conventional mechanical push-buttons for channel selection. Neons can be used to indicate the selected channel, while the latched output of the ML237B drives the varicap tuner via a bias selection network.

A stepping facility is included whereby the application of a suitable negative-going pulse to the step input causes the selected channel output to advance by one.

FEATURES

- 6-Channel Capability
- Direct Neon Drive
- Low Impedance Drive to Varicap
- Uses 33V Varicap Supply
- Remote Control Stepping Facility
- Sound Muting During Selection
- Selected Channel 1 on Power-up
- Channels Are Selected With a Negative (or Earth) Input

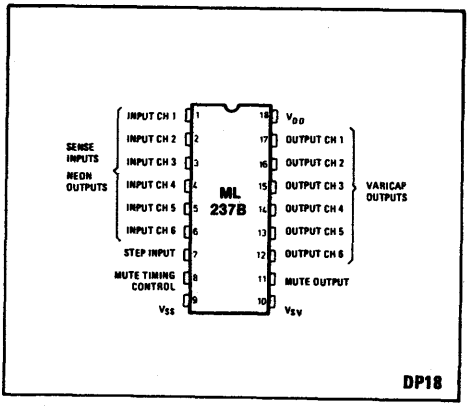


Fig. 1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	−10°C to +65°C
Storage temperature	−10°C to +85°C
Supply, Vss–VDD	36V
Varicap voltage VSV	Vss+0.3V

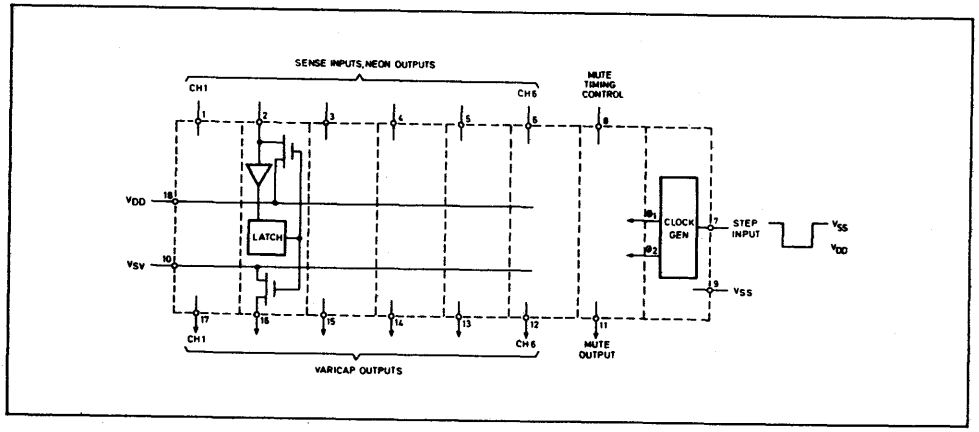


Fig. 2 Functional block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

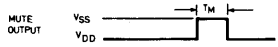
T_{amb} = +25°C, V_{DD} = 0, V_{SS} = V_{SV} = 30V to 36V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input current			1	μA	V_{IN} = V_{SS}
Output leakage			1	μA	V_{OUT} = 0
Mute switch O/P leakage			10	μA	V_{OUT} = 0
Supply current		5	8	mA	
R_{ON} of varicap switch		50	100	Ω	I_{OUT} = 10mA
Step pulse width	0.2			ms	>.05Tm
Neon switch output current			2	mA	
Mute switch R_{ON}		100	200	Ω	I_{OUT} = 5mA
Input threshold	0.4	0.5	0.6	V_{SS}	
Step input current	10		1000	μA	V_{IN} = 0
Mute period		400		ms	C_M = 0.68 μF
Step pulse level	0		V_{SS} −29	V	

NOTES

The mute timing can be increased by using a higher value of capacitor (C_M)

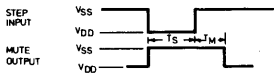
Touch plate selection:



Tm ≃ Cm x 0.6ms/nF

If the channels are selecting by stepping then the mute output is extended by the clock pulse width T_S

Stepping selection:



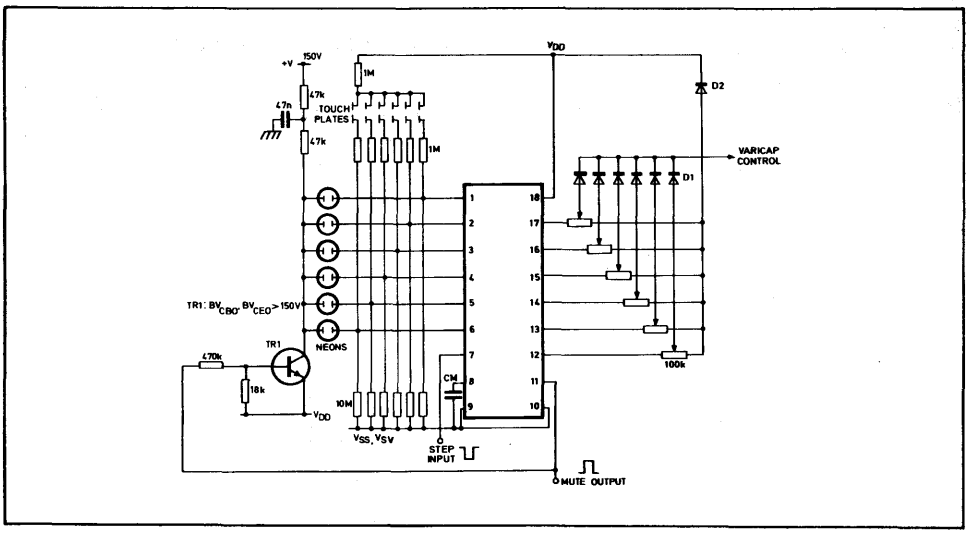


Fig. 3 Typical applications using neons as channel indicators

PLESSEY
Semiconductors

ML238B

8-CHANNEL TOUCH CONTROL INTERFACE

The ML238B is an eight channel sense circuit designed specifically for touch tuning in colour and monochrome television receivers. Using low threshold P-MOS technology, the circuit can be driven directly from two-terminal touch plates – replacing conventional mechanical push-buttons for channel selection. Neons or LEDs may be used to indicate the selected channel, while the latched output of the ML238B drives the varicap tuner via a bias selection network.

A stepping facility is included whereby the application of a suitable negative-going pulse to the step input causes the selected channel to advance by one.

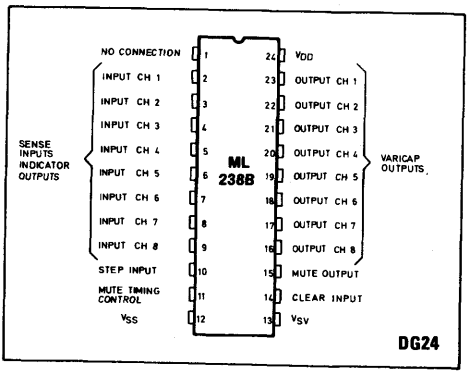


Fig. 1 Pin connections

FEATURES

- 8-Channel Capability
- Direct Neon Drive
- Direct Neon or LED Drive
- Low Impedance Drive to Varicap
- Uses 33V Varicap Supply
- Remote Control Stepping Facility
- Sound Muting During Selection
- Selects Channel 1 on Power-up
- A Negative Pulse on Clear Resets to Channel 1

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	−10°C to +65°C
Storage temperature	−10°C to +85°C
Supply, V_{SS}–V_{DD}	36V
Varicap voltage V_{SV}	V_{SS} +0.3V

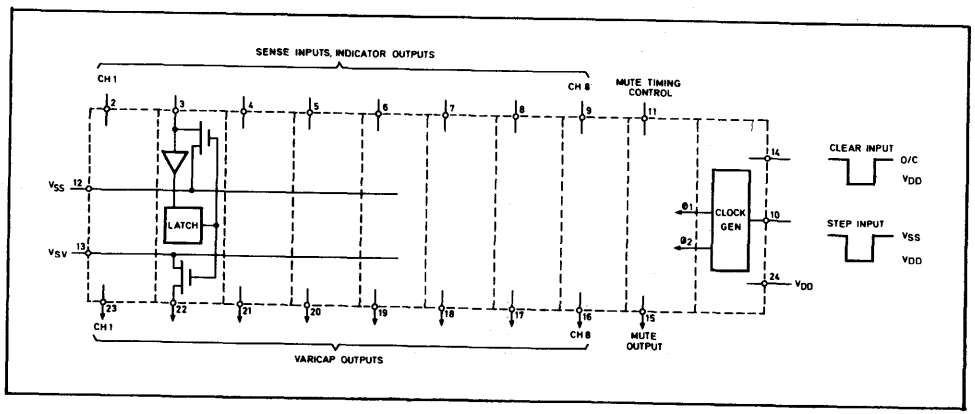


Fig. 2 Functional block diagram

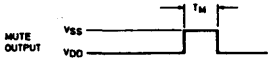
ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 0, V_{SS} = V_{SV} = 30V to 36V

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Output leakage			1	µA	V_{out} = 0
Supply current		6	9	mA	
Input current			1	µA	V_{in} = 0V
R_{ON} of varicap switch		50	100	Ω	I_{OUT} = 10mA
R_{ON} of indicator switch		180	300	Ω	I_{OUT} = 10mA
I/P threshold	0.4	0.5	0.6	V_{SS}	
Step pulse level	0		V_{SS} −29	V	
Ts step pulse width	0.2			ms	>.0 5 Tm
Clear pulse level	0		V_{SS} −29	V	
Clear pulse width	0.2			ms	
R_{ON} of mute switch		100	200	Ω	I_{OUT} = 5mA
T_m mute timing		400		ms	Cm = 0.68µF
Step I/P current	10		1000	µA	V_{in} = 0
Mute O/P leakage			10	µA	V_{OUT} = 0

NOTES:
The mute timing can be increased by using a higher value of capacitor (C_m) (See Fig. 4).

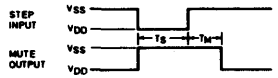
Touch plate selection:



$T_m \simeq C_m \times 0.6ms/nF$

If the channels are selecting by stepping then the mute output is extended by the clock pulse width T_s.

Stepping selection:



The clear I/P should be left open circuit when not in use.

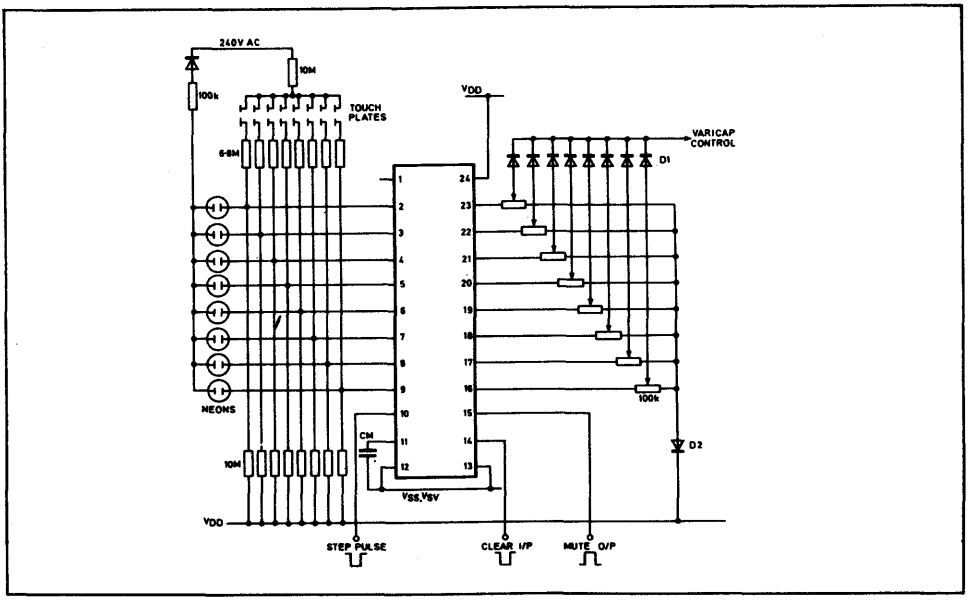


Fig. 3 Typical applications using neons as channel indications

APPLICATION NOTES

Application using LEDs as channel indicators

In applications where the use of mains is not desired channel selection can be made by using the +30V Vss supply as a compromise but at the expense of reduced input sensitivity. In this case LEDs can be used as channel indicators.
The 1.2kΩ and 820Ω resistors limit the LED current to 10mA, whilst the diode ensures less than 1μA leakage when the LED is reverse biased. It is desirable to have a 1MΩ resistor between the touch plates and the input as a safeguard against static.
On selection of a channel, the potential divider chain comprising the 1MΩ resistor, the finger resistance and the 10MΩ resistor sets the threshold voltage on the input pin. When the channel is selected the IC provides a current source to the LED.

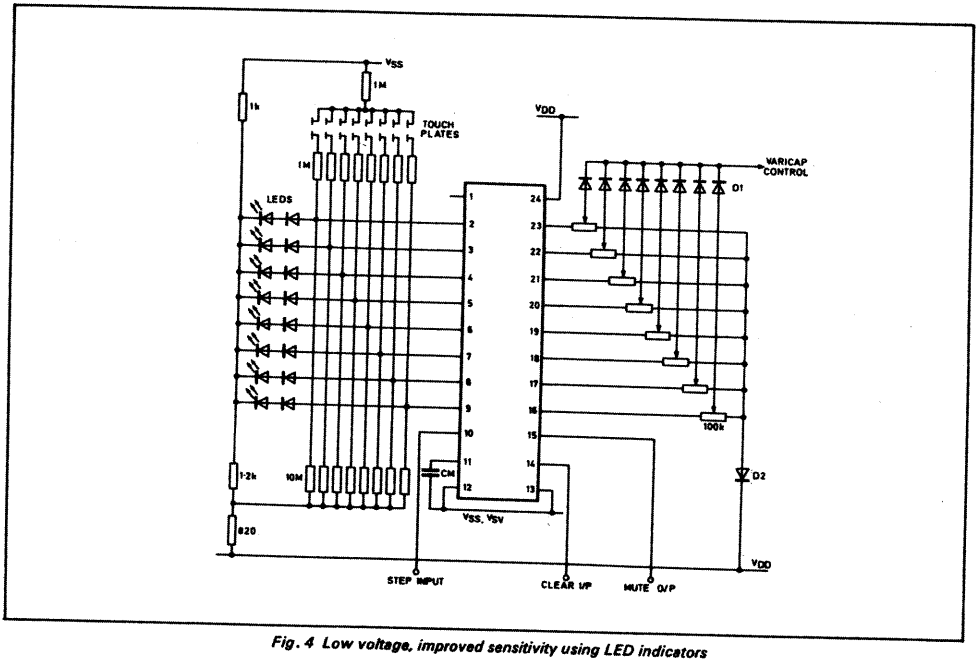


Fig. 4 Low voltage, improved sensitivity using LED indicators

PLESSEY
Semiconductors

ML239B

8 – CHANNEL TOUCH CONTROL INTERFACE

The ML239B is an eight channel sense circuit designed specifically for touch tuning in colour and monochrome television receivers. Using low threshold P-MOS technology, the circuit can be driven directly from two-terminal touch plates – replacing conventional mechanical push-buttons for channel selection. Neons can be used to indicate the selected channel, while the latched output of the ML239B drives the varicap tuner via a bias selection network.

A stepping facility is included whereby the application of a suitable negative-going pulse to the step input causes the selected channel output to advance by one.

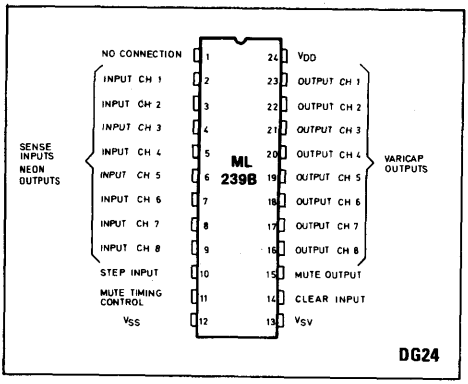


Fig. 1 Pin connections

FEATURES

- 8-Channel Capability
- Direct Neon Drive
- Low Impedance Drive to Varicap
- Uses 33V Varicap Supply
- Remote Control Stepping Facility
- Sound Muting During Selection
- Selects Channel 1 on Power-up
- A Negative Pulse on Clear Resets to Channel 1
- Channels are Selected with a Negative (or Earth) Input

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	−10°C to +65°C
Storage temperature	−10°C to +85°C
V_{SS}–V_{DD} supply	36V
Varicap voltage V_{SV}	V_{SS} +0.3V

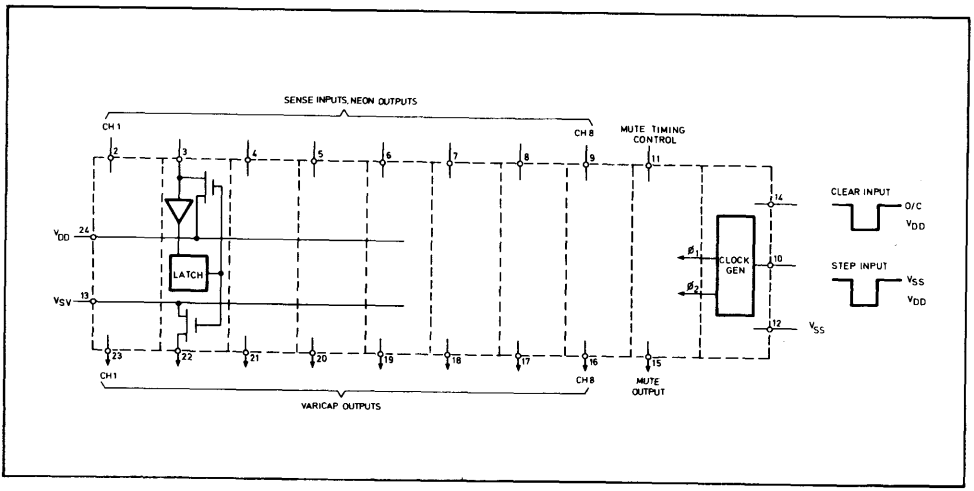


Fig. 2 Functional Block Diagram

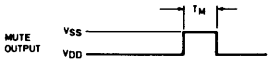
ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 0, V_{SS} = V_{SV} = 30V to 36V

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Step, clear pulse level	0		V_{SS} −29	V	
Input current			1	µA	V_{IN} = V_{SS}
Output leakage			1	µA	V_{OUT} = 0
Mute switch O/P leakage			10	µA	V_{OUT} = 0
Supply current		6	9	mA	
R_{ON} of varicap switch		50	1000	Ω	I_{OUT} = 10mA
Clear step pulse width	0.2			ms	>.05Tm
Neon switch output current			2	mA	
R_{ON} of mute switch		100	200	Ω	I_{OUT} = 5mA
Input threshold	0.4	0.5	0.6	V_{SS}	
Step input current	10		1	mA	V_{IN} = 0
Mute period		400		ms	C_M = 0.68µF

NOTES:
The mute timing can be increased by using a higher value of capacitor (C_m)

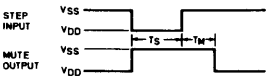
Touch plate selection:



$T_m \simeq C_m \times 0.6ms/nF$

If the channels are selecting by stepping then the mute output is extended by the clock pulse width T_s.

Stepping selection:



The clear I/P should be left open circuit when not in use.

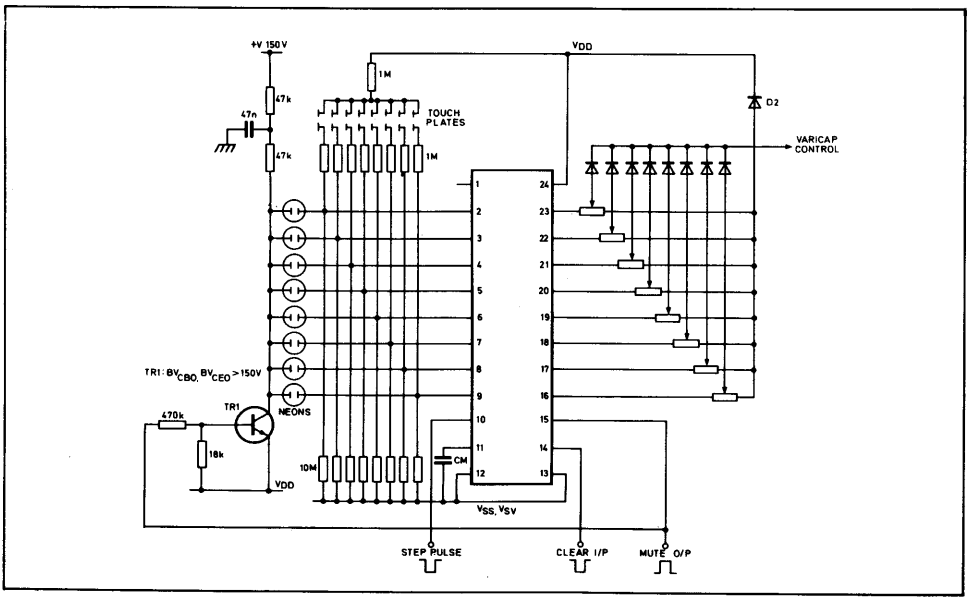


Fig. 3 Typical applications using neons as channel indications

PLESSEY
Semiconductors

ML920
REMOTE CONTROL RECEIVER

Plessey Semiconductors have developed and produced a range of monolithic integrated circuits which give a wide variety of remote control facilities. As well as ultrasonic or infra red transmission, cable, radio or telephone links may also be utilised. Pulse position modulation (PPM) is used with or without carrier and automatic error detection is also incorporated. Although initially designed with TV remote control in mind the devices may equally easily be applied for use in radios, tuners, tape and record decks, lamps and lighting, toys and models, industrial control and monitoring.

The ML920 demodulates the PPM signal received from the SL490 transmitter. After error checking the received code may condition a 20 programme memory or one of three D/A converters.

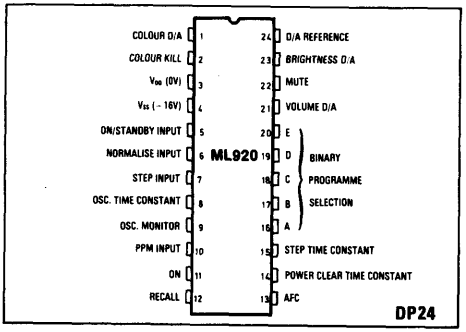


Fig. 1 Pin connections

QUICK REFERENCE DATA

- Power supply: 16V 14mA
- Demodulation: Pulse position with time window checking by on-chip oscillator
- Decoder: 5 bit with successive codeword comparison
- Programme: Latched 5 bit binary, 20 programmes
- Analogue controls: 3 static current mirror converters, 32 step with normalise level
- Other outputs: On, Recall Display, AFC, Mute, Colour Kill, Oscillator Monitor
- Local inputs: On/Standby, Step, Normalise

FEATURES

- Accepts 5 Bit PPM
- All Timing From On-Chip Oscillator
- Incorporates Error Protection
- Easily Used With Ultrasonic or Infra-red System
- Up to 20 Programmes With Latched Binary Output
- 3 D/A Outputs With Normalise Level At $\frac{3}{8}$ of Max.
- Automatic Power-On Reset and Normalise
- Many Other Facilities, AFC, Mute, Colour Kill, Recall etc.

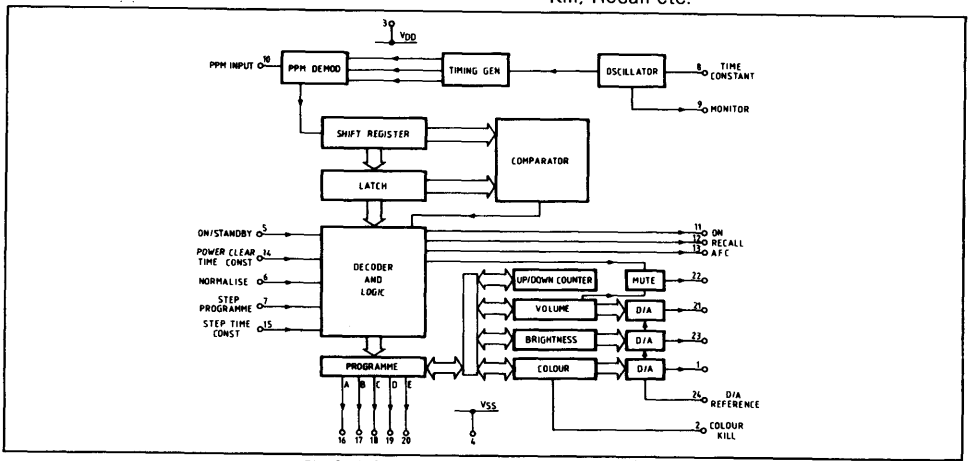


Fig. 2 ML920 remote control receiver block diagram

ELECTRICAL CHARACTERISTICS (see Fig. 3)

Test conditions (unless otherwise stated):
V_{SS}= 0V
V_{DD} = −16V
T_{amb} = 25°C

Characteristics	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	3	14		18	V	
Supply current	3		8	14	mA	
Input logic level high	5, 6, 7,	−1		0	V	
low		V_{DD}		V_{DD} +3.5	V	
Output logic level high	2, 11-13, 16-20, 22	−1		0	V	50k to V_{DD}
low		V_{DD}		V_{DD} +0.5	V	50k to V_{DD}
Analogue output current range (pins 1, 21, 23)	1, 21, 23	0		$\frac{31}{8}$	I_{REF}	3.9k to V_{DD}
Analogue step size	1, 21, 23	0	$\frac{1}{8}$	$\frac{1}{4}$	I_{REF}	V_{out} < V_{DD} +5V
D/A reference, I_{REF}	24	−250	−345	−455	µA	33k to V_{DD}
Oscillator timing	9		1.5k		Hz	C = 22n, R=100k See note 1
Power clear time constant	14		400		ms	C = 4.7µ R=100k
Step time constant	15		1		s	C = 470n R = 3.3M
Monitor output 'high'	9	−1		0	V	Internal load
'low'		V_{DD}		V_{DD} +0.5	V	provided
PPM input logic level high		-1		0	V	
PPM input logic level low	10	V_{DD}		-6	V	
PPM input pulse width		1		$22T_{osc}$	µs	$T = \frac{1}{f_{osc}}$

Note 1. R_{osc} (Pin 8) is 47k - 200kΩ, 2fmon (Pin 9) = $f_{osc} \simeq \frac{1}{0.15CR}$

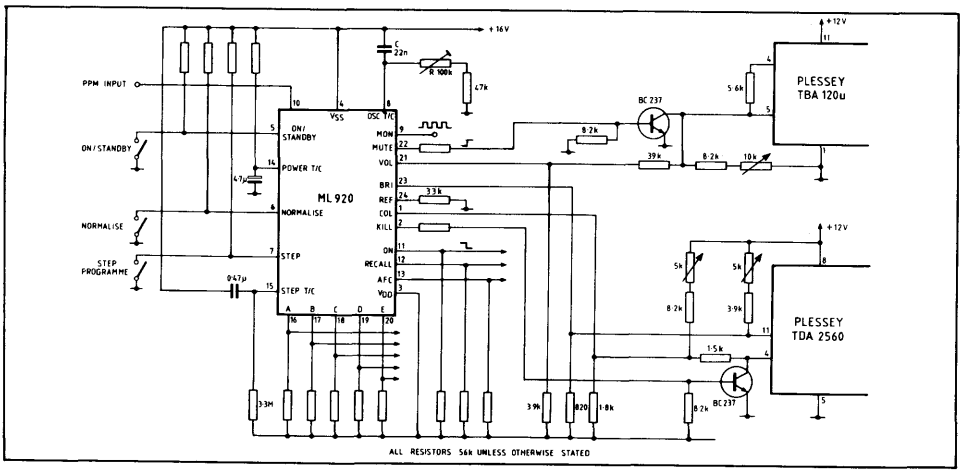


Fig. 3 PPM receiver application

PIN FUNCTIONS

Negative Logic: 0 is 0V (V_{SS}), 1 is −17V (V_{DD})

1, 21, 23. Colour, Volume, Brightness
These three outputs are from three 5 bit current mirror D/A converters. They are referenced to the current drawn from pin 24, I_{ref}, and give 32 steps, $I_{ref}/8$ per step, from 0 to 31/8 I_{ref}. The outputs will be set to 12/8 I_{ref} by the NORMALISE input, the normalise code from the transmitter, or when the ON output goes to a 1.

2. Colour kill
This output gives a logic 0 when the COLOUR D/A output is zero.

3. V_{DD}
−17V power supply

4. V_{SS}
0V power supply

5. On/Standby input
A 1 on this pin will toggle pin 11 (ON O/P), generate

RECALL and AFC, normalise VOLUME, BRIGHTNESS and COLOUR, reset MUTE and set channel code 00000.

6. Normalise input

A 1 will normalise the VOLUME, BRIGHTNESS and COLOUR outputs. A RECALL signal is generated and MUTE is reset.

7. Channel step

The channel code will step up by 1 as long as this pin is held at logic 1. The time period between steps is defined by an RC constant attached to pin 15. On reaching 20 the next step returns to 1. On output is set to ON, and AFC is generated. If the TV goes from Standby to ON, RECALL is generated and VOLUME, BRIGHTNESS and COLOUR are normalised. If VOLUME is not 0, MUTE is reset.

8. Oscillator time constant

An RC time constant is formed for the clock timing by connecting external components, one resistor and one capacitor, to this pin. Adjusted so that period of output on pin 9 is 1/20 of 0 interval of incoming PPM.

9. Oscillator monitor

This output is a division of two of the oscillator, and and is available for testing and setting purpose.

10. PPM I/P

The output of the front end amplifier is connected here such that the signal is in the form of positive pulses separated by time periods whose length define the data. With no signal, PPM input is at a logic 1.

11. On O/P

Open drain output. Logic 1 denotes TV set ON: Logic 0 TV set standby. Set to 1 when channel number changes. Set to 0 by power clear or by transmitter selected Standby. Toggle to opposite state by manual ON/STANDBY control.

12. Recall O/P

Open drain output. A 1 may be used to trigger an on-screen display. A static output is generated by the manual controls ON/STANDBY and NORMALISE.

A pulse is generated by any channel change if the circuit switches to ON at the time, and by RECALL and NORMALISE commands from the transmitter.

13. AFC O/P

Open drain output. Logic 1 can inhibit the tuner AFC.

A static output is generated by manual ON/STANDBY control. A pulse is generated by any channel number change.

14. Power clear

A capacitor and resistor connected here define the time delay for the power clear circuit, which normalises all D–A outputs etc.

15. Channel step time constant

An R–C time constant defines the time period between increments of the channel number when stepping.

16–20. Channel outputs

5 Outputs encode 20 channel numbers in binary code

EDCBA
Channel 1 is 00000
Channel 20 is 10011

E is first and A is last in the PPM pulse train.
Channel 1 is set when ON goes to a 1

21. Volume.

See Pin 1

22. Mute O/P

This will change state (toggle) on reception of a mute command and if VOLUME O/P is zero MUTE O/P is held at 0.

23. Brightness

See Pin 1

24. D/A Reference

A current drain I_{ref}, set by a single external resistor will set the nominal step of the D/A outputs to $I_{ref}/8$.

Transmitter code	Function
EDCBA	
00000	Programme 1
00001	Programme 2
00010	Programme 3
00011	Programme 4
00100	Programme 5
00101	Programme 6
00110	Programme 7
00111	Programme 8
01000	Programme 9
01001	Programme 10
01010	Programme 11
01011	Programme 12
01100	Programme 13
01101	Programme 14
01110	Programme 15
01111	Programme 16
10000	Programme 17
10001	Programme 18
10010	Programme 19
10011	Programme 20
10100	Colour +
10101	Programme Step +
10110	Volume +
10111	Brightness +
11000	Standby
11001	Mute
11010	Recall
11011	Normalise
11100	Colour –
11101	Programme Step –
11110	Volume –
11111	Brightness –

Table 1 Basic 32 command set

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V).

Supply Voltage V_{DD}	+0.3V to –25V
Voltage at any input	+0.3V to –25V
Operating voltage range, V_{DD}	–14V to –18V
Maximum power dissipation	600mW
Operating temperature range	–10°C to +65°C
Storage temperature range	–55°C to +125°C

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ML922

REMOTE CONTROL RECEIVER

Plessey Semiconductors have developed and produced a range of monolithic integrated circuits which give a wide variety of remote control facilities. As well as ultrasonic or infra red transmission, cable, radio or telephone links may also be utilised. Pulse position modulation (PPM) is used with or without carrier and automatic error detection is also incorporated. Although initially designed with TV remote control in mind the devices may equally easily be applied for use in radios, tuners, tape and record decks, lamps and lighting, toys and models, industrial control and monitoring.

The ML922 demodulates the PPM signal received from the SL490 transmitter. After error checking the received code may condition a 10 programme memory or one of three D/A converters.

The receiver timing may be set by adjusting the oscillator time constant to give 40 periods at pin 6 equal to a 0 interval on the received PPM input..

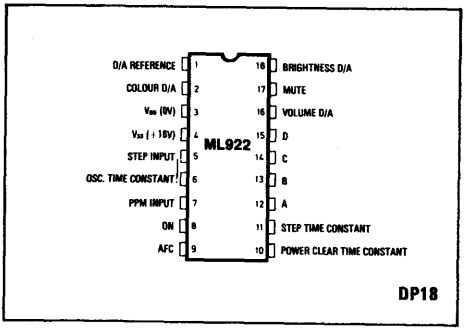

Fig. 1 Pin connections

FEATURES

- Accepts 5 Bit PPM
- All Timing From On-Chip Oscillator
- Incorporates Error Protection
- Easily Used With Ultrasonic or Infra-red System
- Up to 10 Programmes With Latched Binary Output
- 3 D/A Outputs With Normalise Level At $\frac{3}{8}$ of Max.
- Automatic Power-On Reset and Normalise
- Many Other Facilities, AFC, Mute, Etc.

QUICK REFERENCE DATA

- Power supply: 16V 14mA
- Demodulation: Pulse position with time window checking by on-chip oscillator
- Decoder: 5 bit with successive codeword comparison
- Programme: Latched 4 bit binary, 10 programmes
- Other outputs: On, AFC, Mute
- Local inputs: Programme step

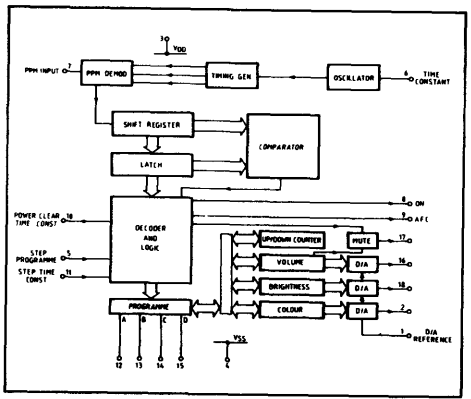

Fig. 2 ML922 remote control receiver block diagram

Transmitter code EDCBA	Function
0000X	Programme 1
0001X	Programme 2
0010X	Programme 3
0011X	Programme 4
0100X	Programme 5
0101X	Programme 6
0110X	Programme 7
0111X	Programme 8
1000X	Programme 9
1001X	Programme 10
10100	Analogue 1 +
10101	Programme Step +
10110	Analogue 2 +
10111	Analogue 3 +
11000	Standby
11001	Mute (Analogue 2)
11011	Normalise
11100	Analogue 1 −
11101	Programme Step −
11110	Analogue 2 −
11111	Analogue 3 −

Table 1 Basic 21 command set for ML922

ELECTRICAL CHARACTERISTICS (see Fig. 3)

Test conditions (unless otherwise stated):
$V_{SS} = 0V$
$V_{DD} = -16V$
$T_{amb} = 25°C$

Characteristic	Pin	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply voltage	3	14		18	V	
Supply current	3		8	14	mA	
Input logic level high	5	−1		0	V	
low		V_{DD}		$V_{DD}+3.5$	V	
Output logic level high	8, 9, 12-15, 17	−1		0	V	50k to V_{DD}
low		V_{DD}		$V_{DD}+0.5$	V	50k to V_{DD}
Analogue output current range	2, 16, 18	0		$\frac{31}{8}$	I_{ref}	3.9k to V_{DD}
Analogue step size	2, 16, 18	0	$\frac{1}{8}$	$\frac{1}{4}$	I_{ref}	$V_{out} < V_{DD} + 5V$
D/A reference, I_{REF}	1	−250	−345	−455	μA	33k to V_{DD}
Oscillator timing	6		3		kHz	C = 22n, R = 100k See note 1
Power clear time constant	10		400		ms	C = 4.7μ R = 100k
Step time constant	11		2		s	C = 470n R = 3.3M
PPM input logic level high	7	-1		0	V	
PPM input logic level low	7	V_{DD}		-6	V	
PPM input pulse width	7	1		22T_{osc}	μs	

Note 1. $R_{osc.}$ (pin 6) is 25k → 200kΩ. $f_{osc.} \simeq \frac{1}{0.15CR}$

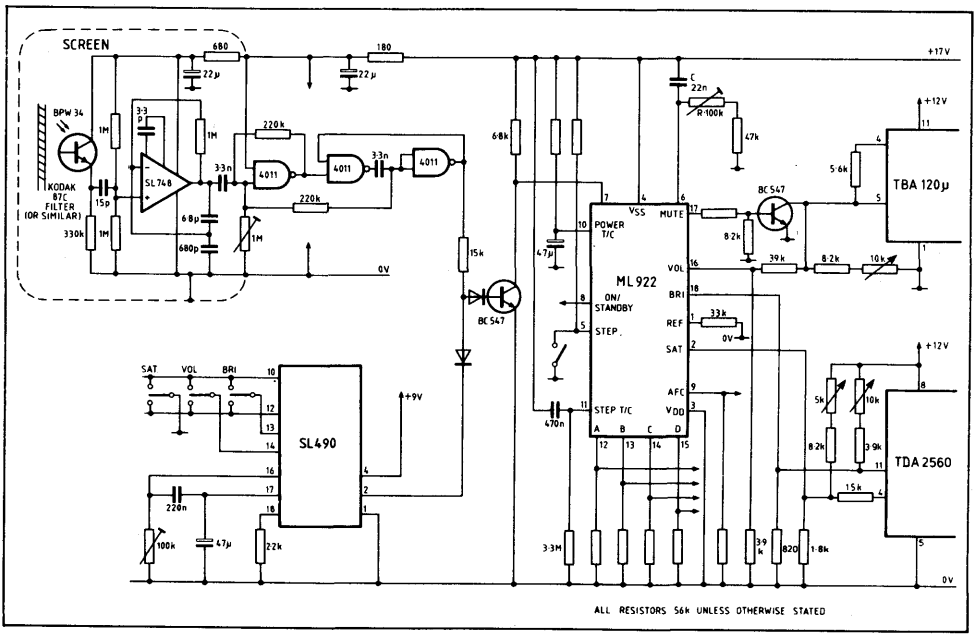

Fig. 3 PPM infra-red receiver application with local up/down controls using a directly connected SL490

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V).

Supply Voltage V_{DD}	+0.3V to −25V
Voltage at any input	+0.3V to −25V
Maximum power dissipation	600mW
Operating temperature range	−10°C to +65°C
Storage temperature range	−55°C to +125°C

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PRELIMINARY INFORMATION

Preliminary Information is issued to advise Customers of potential new products which are designated '*Experimental*' but are, nevertheless, serious development projects. Details given may, therefore, change without notice and no undertaking is given or implied as to current or future availability. Customers incorporating '*Experimental*' product into their equipment designs do so at their own risk. Please contact your local Plessey Semiconductors Sale Office for details of current status.

ML923

REMOTE CONTROL RECEIVER

The ML923 is an MOS/LSI monolithic integrated circuit for use as a receiver of remote control signals for television control. It accepts 24 of the 32 codes transmitted by the SL490 transmitter circuit in the Pulse Position Modulation (PPM) method of coding.

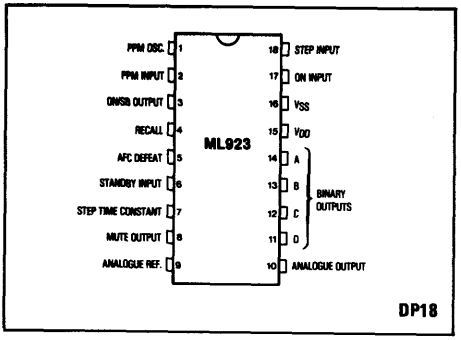


Fig.1 Pin connections

FEATURES

- 16 Channel Selection Codes
- Single Analogue Output
- Mute Output (Toggle)
- On-set Controls—Channel Step, ON, Reset
- Normalise to $\frac{3}{8}$ of Max Output on Analogue Output
- Outputs Provide Control of ON/STANDBY, Analogue Mute, and AFC Defeat
- Choice of Power-Up Function:
  a) Power Up to Standby State, Switch to ON State by Local or Remote Command and STANDBY by Remote Command.
  b) Power Up to ON State, Switch OFF with Solenoid Operated Mains Switch by Local or Remote Command.

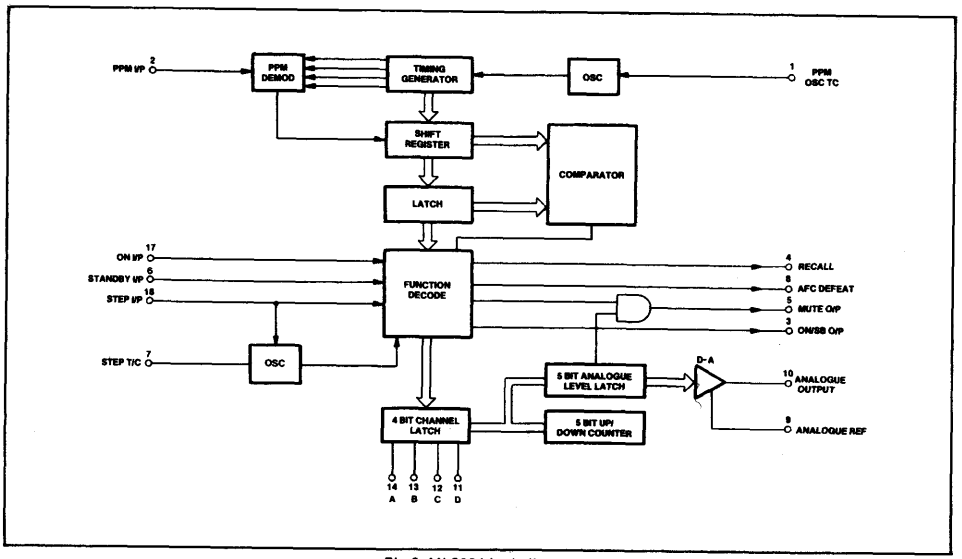


Fig.2 ML923 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$, $V_{SS} = 0V$, $V_{DD} = -16V$

Characteristics	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	1	14		18	V	
Supply current	1		6		mA	
Input logic level high	6, 17, 18	-1		0	V	
Input logic level low		V_{DD}		$V_{DD}+3.5$	V	
Output logic level high	3, 4, 11, 14	-1.5		0V	V	50k to V_{DD}
Output logic level low	8	V_{DD}		$V_{DD}+0.5$	V	
Analogue output current range	10	0		$\frac{31}{8}$	1 Ref	3.9k to V_{DD}
Analogue step size	10	0	$\frac{1}{8}$	$\frac{1}{4}$	1 Ref	$V_{out} < V_{DD}+5V$
D/A reference, I ref	9	-250	-345	-455	mA	33kΩ to V_{DD}
PPM		15		150k	Hz	Typical TC
Oscillator frequency	1		3k		Hz	C = 22nF R = 100kΩ
On input or standby input time constant for power on	6 or 17	250		500	ms	
Step time constant	7		1		s	C = 470nF R = 3.3MΩ
PPM input logic level high ('1')	2	-1		0	V	
PPM input logic level low ('0')	2	V_{DD}		-6	V	
PPM input pulse width	2	1		$22\,T_{osc}$	μs	$T = \frac{1}{f_{osc}}$

Note 1 R_{osc} (pin 5) is 47kΩ - 200kΩ $\quad f_{osc} \simeq \frac{1}{0.15CR}$

OPERATING NOTES

The receiver operates on a timescale fixed by an internal oscillator and its external timing components. The oscillater may be adjusted to any value between 15Hz and 150kHz (allowing different receivers to respond to different transmission rates within the same operating area).

A counter is reset whenever a pulse is received and allowed to count at half the oscillator frequency. For example, taking an oscillator frequency of 1.56kHz:—

Resetting is blocked for the first 14ms and windows from 14ms to 22ms and from 22ms to 40ms determine whether a '1' or a '0' is present. Periods between pulses of 40ms to 80ms are recognised as word intervals. Checks are made to ensure 6 pulses, or 5 bits, are received for a word to be valid, and only after two consecutive and identical words is the receiver allowed to respond to the incoming code. Channel step time period is derived from an external time constant.

PIN FUNCTIONS

Positive Logic: Logic '1' = V_{SS}, 0V Logic '0' = V_{DD}, -16V

1. Oscillator Time Constant An RC Time Constant at this pin defines the internal clock frequency. The clock frequency may be varied from 15Hz to 150kHz.

2. PPM Input The output of the Front End Amplifier is connected to the pin; the signal must consist of a normal logic '0' level with pulses to logic '1', corresponding to the PPM pulse from the transmitter.

3. ON/SB Output Open drain output. Logic '0' denotes onset. Logic '1' standby set. Set to '0' when channel number changes, and by ON input at logic '0', set to '1' by standby input or by transmitter selected OFF.

4. Recall O/P Open drain output. A '0' may be used to trigger an on-screen display. A '0' is output during an input at pin 17, ON input. The pulse to logic '0' is generated by any channel change if circuit switches to ON from Standby, and by recall and normalise commands from the remote transmitter.

5. AFC O/P Open drain output. A logic '0' can inhibit tuner AFC. A static output is generated by manual ON control. A pulse is generated by any channel number change.

6. Standby Input A logic '0' will select standby state and normalise the analogue output to 3/8 maximum and select programme 1. An RC time constant may be connected to select standby at power ON.

7. Channel Step Time Constant An RC time constant defines the time period between increments of the channel number when stepping.

8. MUTE Output This will change state (toggle) on receptin of a Mute command or will remain at logic '1' if the D-A output is zero. The output is reset by any channel change command.

9. Analogue Reference A current drain attached to this input will define the current step of the D-A output. The current is equal to 8 output current steps.

10. Analogue Output The output of a current mirror D-A convertor provides a current source of between 0mA and 1.3mA. It is variable in 32 steps, UP or DOWN. It is normalised to 3/8 maximum value by the ON/SB input, and by normalise command from the transmitter.

11, 12, 13, 14. Channel Selection Outputs These outputs encode the 16 channels in binary code.

	A	B	C	D
Channel 1	0	0	0	0
Channel 16	1	1	1	1

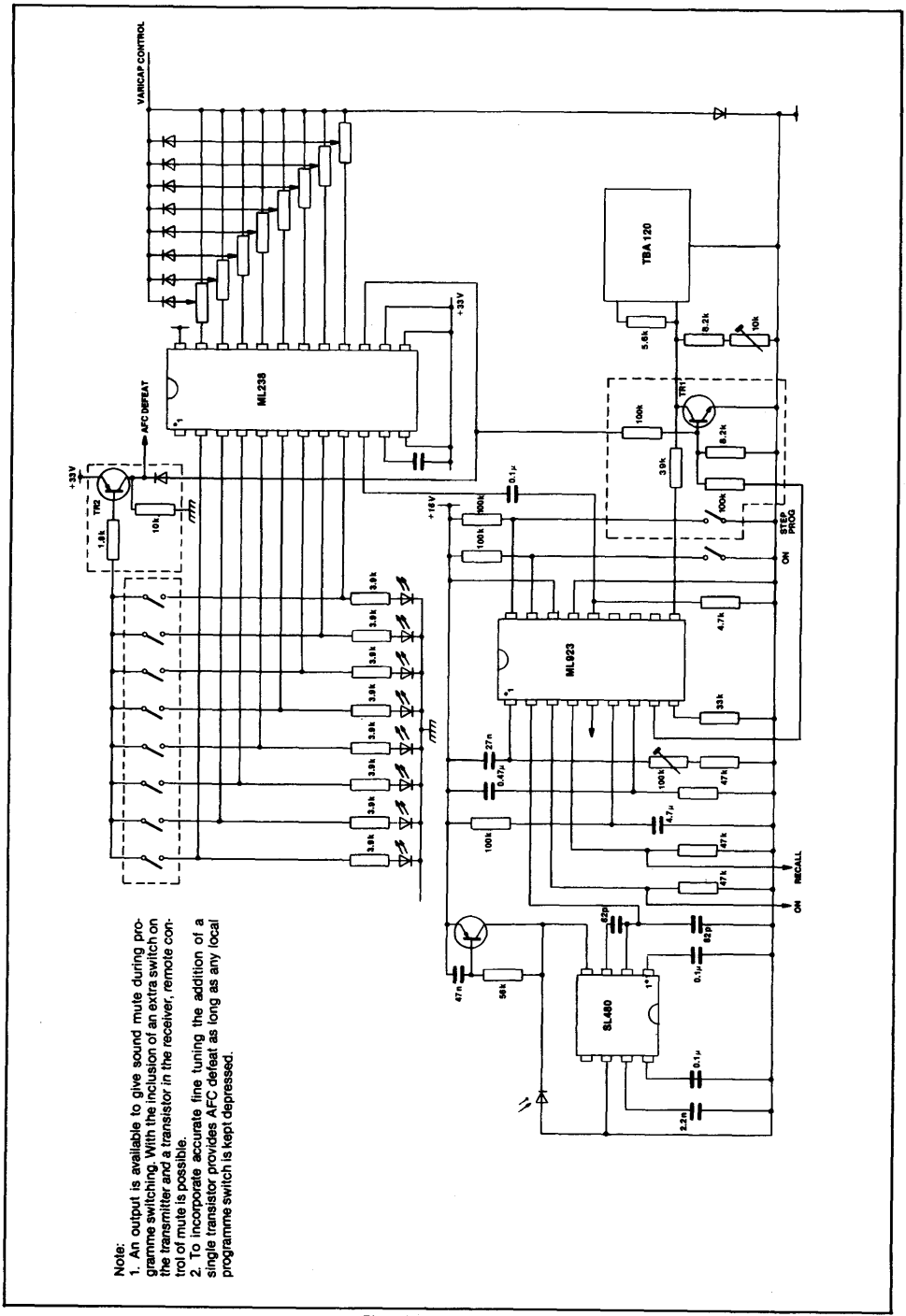
Set to channel 1 on set switch ON.

15. V_{DD} - 14V to - 18V power supply

16. V_{SS} 0V (Ground)

17. ON I/P A logic '0' will switch the ON/SB output to ON (logic '0'). Channel 1 is selected and analogue output is normalised to 3/8 maximum. An RC time constant may be connected to select set ON at power on. The AFC defeat signal is generated and Mute is reset.

18. Step Input The channel code will step up by 1 as long as the pin is held at logic '0'. The time period between steps is defined by an RC constant on pin 10. When the channel code reaches 16 it will go to 1 next step. A step input will set ON/SB output to ON and normalise the analogue output. Mute is reset if analogue = 0.



Note:
1. An output is available to give sound mute during programme switching. With the inclusion of an extra switch on the transmitter and a transistor in the receiver, remote control of mute is possible.
2. To incorporate accurate fine tuning the addition of a single transistor provides AFC defeat as long as any local programme switch is kept depressed.

Fig.3 Receiver application

CODE					FUNCTION
E	D	C	B	A	
0	0	0	0	0	Channel 1
0	0	0	0	1	Channel 2
0	0	0	1	0	Channel 3
0	0	0	1	1	Channel 4
0	0	1	0	0	Channel 5
0	0	1	0	1	Channel 6
0	0	1	1	0	Channel 7
0	0	1	1	1	Channel 8
0	1	0	0	0	Channel 9
0	1	0	0	1	Channel 10
0	1	0	1	0	Channel 11
0	1	0	1	1	Channel 12
0	1	1	0	0	Channel 13
0	1	1	0	1	Channel 14
0	1	1	1	0	Channel 15
0	1	1	1	1	Channel 16
1	0	1	0	1	Channel Step +
1	0	1	0	0	Analogue +
1	1	0	1	0	Recall
1	1	0	0	1	Mute (Toggle)
1	1	0	1	1	Normalise
1	1	0	0	0	OFF
1	1	1	0	1	Channel Step-
1	1	1	0	0	Analogue-

Table 1 Command set

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PRELIMINARY INFORMATION

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ML924

REMOTE CONTROL RECEIVER

The ML924 is an MOS/LSI integrated circuit for use as a receiver of remote control signals generated by the SL490 transmitter circuit, using PPM (Pulse Position Modulation) encoding technique. The receiver has 5 digital outputs whose response to PPM codes may be programmed by six control lines. It has a handshake interface which provides communication with microprocessors and computers.

FEATURES

- 5 Open drain outputs with enable
- Handshake or interrupt microprocessor and computer interface signals
- On-Chip oscillator
- 6 control lines to programme output response
- 3 selectable output modes

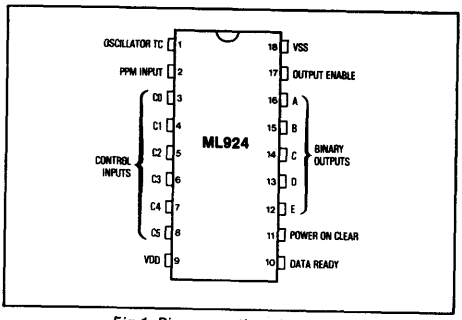

Fig.1 Pin connections (top view)

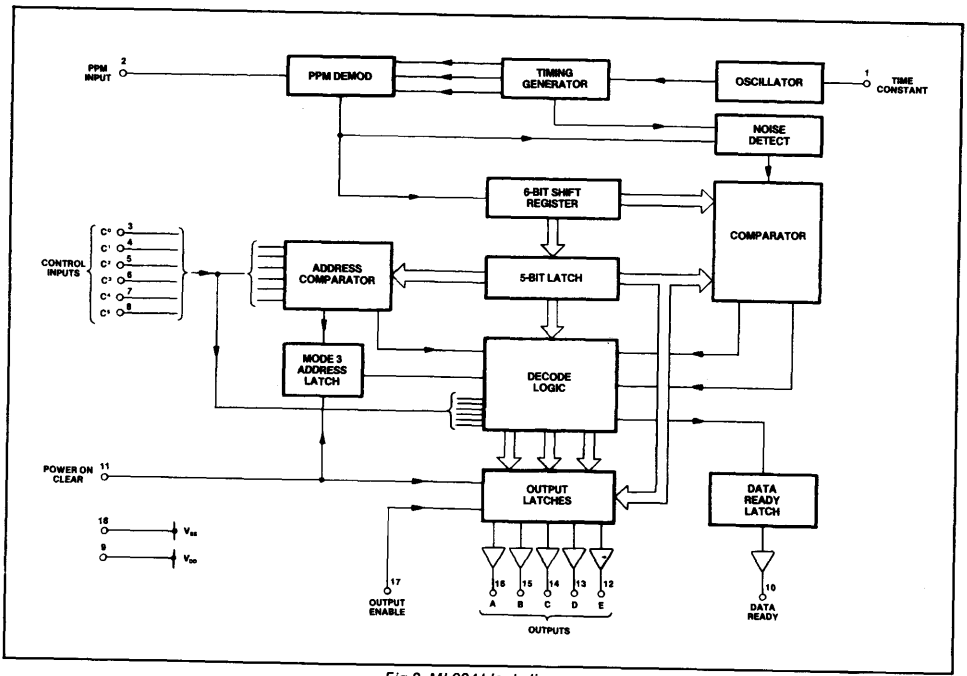

Fig.2 ML924 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
VSS = 0V; VDD = -16V; T_{amb} = +25°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	9	12		18	V	
Supply current	9		6		mA	
Input logic level high ('1')	3-8, 17	-1		0	V	
Input logic level low ('0')		VDD		VDD + 3.5	V	
Output logic level high ('1')	10, 12-16	-1		0V		50k to VDD
Output logic level low ('0')		VDD		VDD + 0.5	V	
Oscillator frequency	1	15	3k	150k	Hz	Typical TC: C = 22nF, R = 100kΩ
PPM input logic level high ('1')	2	-1		0V		
PPM input logic level low ('0')		VDD		-6V		
PPM input pulse width	2	1		22Tosc	s	$T = \frac{1}{fosc}$
Power clear time constant	11	1	400		ms	

NOTE

Rosc (Pin 1) is 56kΩ to 150kΩ, fosc $\simeq \frac{1}{0.15\,CR}$

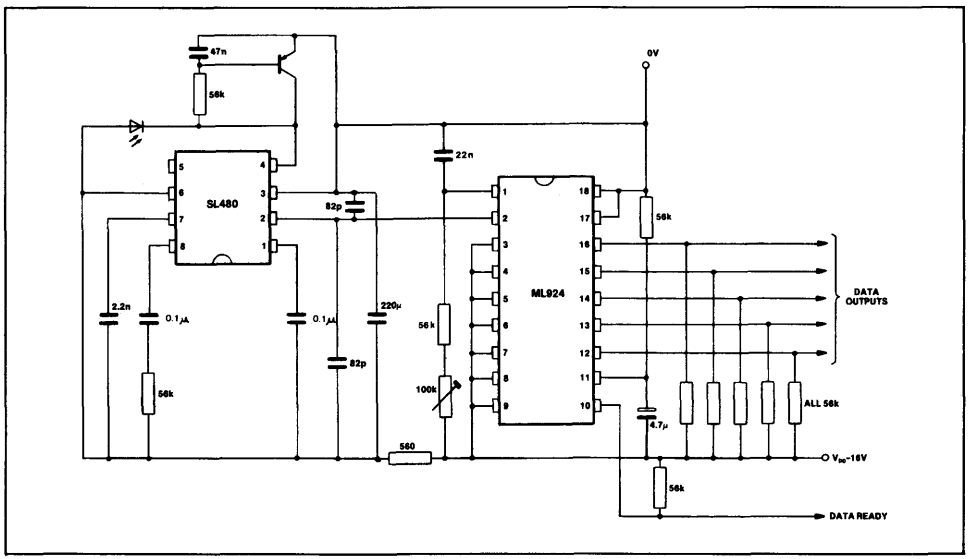

Fig.3 Application for receiving 32 codes from SL490 transmitter. Latched outputs.

PIN FUNCTIONS

Positive Logic: Logic '1' = V_{SS}, 0V Logic '0' = V_{DD}, -16V

1. Oscillator TC An RC time constant at this pin defines the internal clock frequency. The clock frequency may be varied from 15Hz to 150kHz.

2. PPM Input The output of the Front End Amplifier is connected to this pin; the signal must consist of a normal logic '0' level with pulses to logic '1'.

3-8. Control Word C_0 to C_5 Six control bits form the control word which programs the response of the five outputs (see Table 1).

9. V_{DD} -12V to -18V Power Supply.

10. Data Ready Open drain output. An output of logic '1' indicates the reception of a valid PPM word. It will remain at logic '1' for the duration of transmission.

11. Power Clear A capacitor and resistor connected to this pin define the time delay for the Power Clear Circuit.

12-16. Outputs E-A Open drain outputs which respond to the PPM input as defined in Table 1.

17. Output Enable A logic '1' will enable outputs A to E. A logic '0' will turn all outputs off.

18. V_{SS} 0V (Ground).

OPERATING NOTES

The receiver operates on a time scale fixed by an internal oscillator and its external timing components. The oscillator may be adjusted to any value between 15Hz and 150kHz (allowing different receivers to respond to different transmission rates within the same area).

A counter is reset whenever a pulse is received and allowed to count at half the oscillator frequency. For example, at an oscillator frequency of 1.5kHz, resetting is blocked for the first 14ms and windows from 22ms to 40ms determine whether a '1' or a '0' is present. Periods between pulses of 40ms to 80ms are recognised as word intervals. Checks are made to ensure 6 pulses of 5 bits, are received for a word to be valid, and only after two consecutive and identical words is the receiver allowed to respond to the incoming code.

By means of the six control lines, the outputs can respond to the PPM input data in three ways:

1. 5 bit binary output with combinations of latched or momentary responses as shown in table 1.

2. 4 independant outputs with combinations of latched or momentary output as shown in table 1. Any output on 1 or 4 receivers can be addressed by each PPM word.

3. The PPM word can be an address or data depending on the logic state of bit **e**. If PPM bit **e** is '0', the remaining four bits (**a, b, c** and **d**) select one of 16 receivers. If bit **e** is '1', bits **a** to **d** control the outputs A to D. Outputs can be all latched or all momentary.

Control Word						Control Mode	Output Response					Interpretation of PPM Words									
C5	C4	C3	C2	C1	C0		E	D	C	B	A	e	d	c	b	a	e	d	c	b	a
0	0	0	0	0	0	1	LA	LA	LA	LA	LA	E	D	C	B	A					
0	0	0	0	0	1	1	LA	LA	LA	LA	M	PPM decoded on all outputs immediately									
0	0	0	0	1	1	1	LA	LA	LA	M	M										
0	0	0	1	1	1	1	LA	LA	M	M	M										
0	0	1	1	1	1	1	LA	M	M	M	M										
0	1	1	1	1	1	1	M	M	M	M	M										
0	0	1	0	Z	Z	2	—	S/R	S/R	S/R	S/R	0	Y	Y	Z	Z	1	Y	Y	Z	Z
0	1	0	0	Z	Z	2	—	S/R	S/R	S/R	M	Output address		Receiver address			Output address		Receiver address		
0	1	0	1	Z	Z	2	—	S/R	S/R	M	M	Resets an S/R type output					Sets an S/R type output or pulses a momentary output				
0	1	1	0	Z	Z	2	—	S/R	M	M	M										
1	0	Z	Z	Z	Z	3	—	LA	LA	LA	LA	0	Z	Z	Z	Z	1	D	C	B	A
1	1	Z	Z	Z	Z	3	—	M	M	M	M	Address mode		Receiver address			Data mode	PPM data sent to outputs of addressed receiver			

Table 1

NOTES:

1. Control Mode 1: Direct Response to the PPM Code
2. Control Mode 2: ZZ is a 2 bit address for the receiver
   YY selects one of 4 outputs

YY	OUTPUT
00	A
01	B
10	c
11	D

3. Control Mode 3: ZZZZ is a 4 bit address that programmes which transmitter code will select the receiver. If PPM bit **e** = '1', the rest of the PPM word will be read as data. If PPM bit **e** = '0' the rest of the PPM word will be read as an address.

ABSOLUTE MAXIMUM RATINGS

VDD supply and all inputs wrt VSS	+0.3V to −25V
Storage temperatures	−55°C to +125°C
Operating temperature ambient	−10°C to +65°C

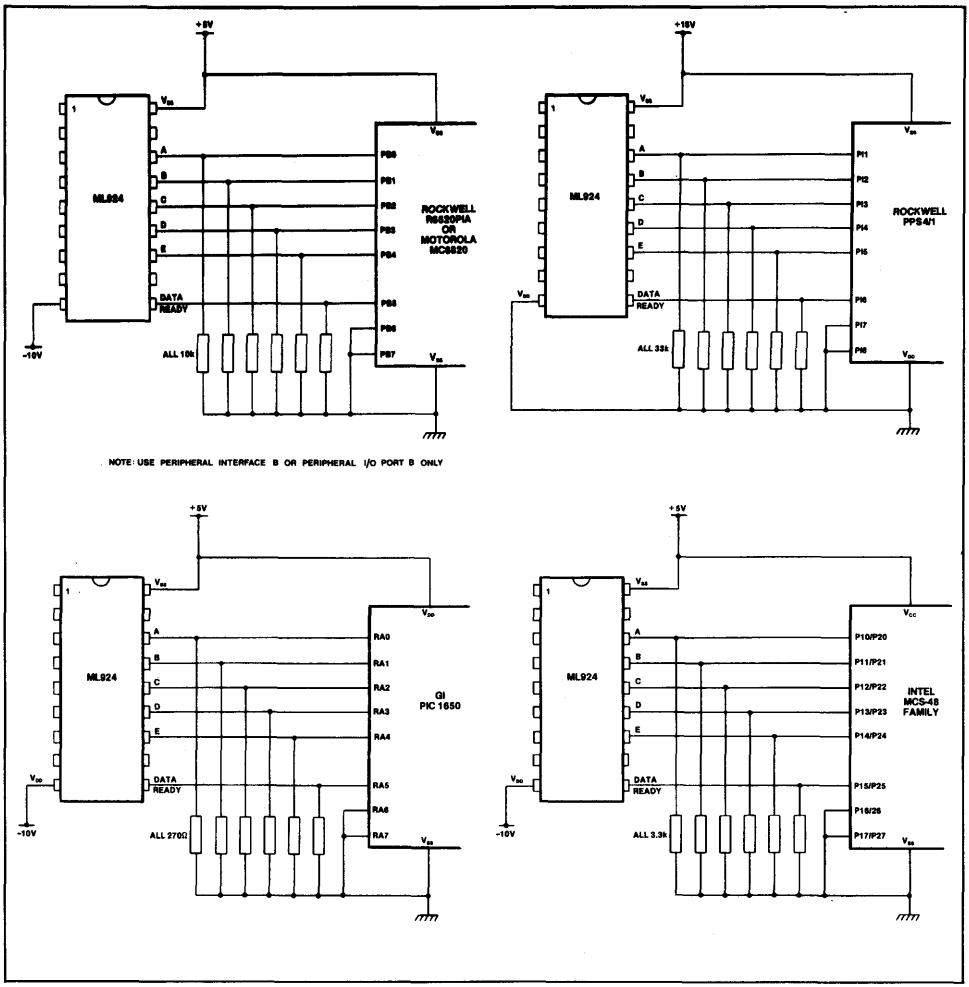

Fig.4 Interface to commonly used microprocessors

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ML925

REMOTE CONTROL RECEIVER FOR TOYS

The ML925 is an MOS/LSI integrated circuit for use as a decoder of PPM remote control commands transmitted by the SL490 or SL491 circuit. It is designed to control either a toy vehicle with two-speed drive motor and a three position latching steering system, or a vehicle with momentary action steering and a third motor, typically a winch. This second vehicle type also has four selectable speeds. Both types have horn, headlights, hazard flasher and turn indicator facilities.

The circuit can operate on the first set of 16 SL490 commands or the second set of 16, thus giving simultaneous control of two independent vehicles with the same integrated circuit type in both.

FEATURES

- Multifunction Toy Control
- High Power, Free Drain Buffers on all Outputs
- Uses Well-Proven High Security PPM Coding with Double Word Checking
- Minimum Component Interfaces Required to Motors and Lamps
- Direct Connection to SL480 Infra-red Preamplifier

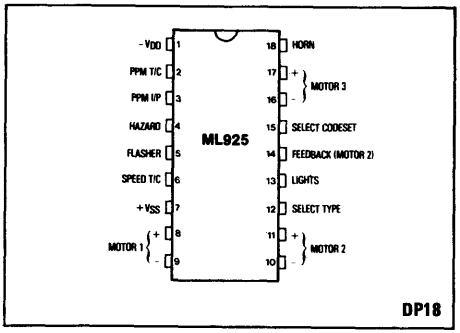

Fig.1 Pin connections

ABSOLUTE MAXIMUM RATINGS

V_{DD} supply inputs with respect to V_{SS}	+0.3V to -25V
Storage temperature	-55°C to +125°C
Operating ambient temperature	-10°C to +65°C

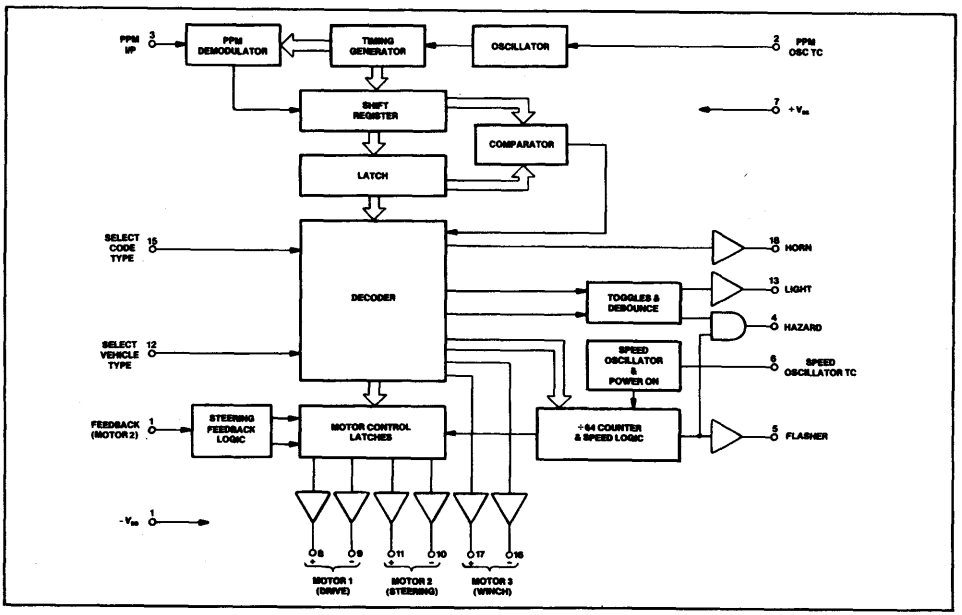

Fig.2 ML925 block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
$T_{amb} = +25°C$, $V_{SS} = 0V$, $V_{DD} = -15V$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage, V_{DD}	1	-12	-15	-18	V	
Supply current	1		8	12	mA	
PPM input high	3	-1		0	V	
low	3	V_{DD}		-6	V	
Code or type select high	12, 15	-1		0	V	
low	12, 15	V_{DD}		-10	V	
Steering feedback, speed time	6, 14	-2.5	-3	-3.5	V	
Constant threshold						
Output voltage motor drives	8-11 16, 17		-0.2	-0.5	V	Output current = 10mA
other drives	4, 5 13, 18		-0.2	-0.5	V	Output current = 5mA
Output leakage all outputs				1	μA	Output voltage = -15V
PPM oscillator frequency	2	15		150k	Hz	
			4		kHz	C = 33nF, R = 50kΩ
Speed control oscillator	6		50		Hz	R_{pos} = 120k, R_{neg} = 270kΩ, C = 100nF
Flasher rate	5		0.8		Hz	For pin 6 as above
PPM input pulse width	3	1		22T	μs	T = 1/f at pin 2

TRANSMITTER CODES					VEHICLE TYPE	
E	D	C	B	A	TYPE A, 'CAR'	TYPE B, 'TRUCK'
X	0	0	0	0	STOP	STOP
X	0	0	0	1	FORWARD STRAIGHT	FORWARD
X	0	0	1	0	REVERSE STRAIGHT	REVERSE
X	0	0	1	1	HORN (MOMENTARY)	HORN (MOMENTARY)
X	0	1	0	0	NOT USED	NOT USED
X	0	1	0	1	FORWARD LEFT	STEER LEFT (MOMENTARY)
X	0	1	1	0	REVERSE LEFT	'WINCH IN' (MOMENTARY)
X	0	1	1	1	FLASHER ON/OFF	FLASHER ON/OFF
X	1	0	0	0	NOT USED	NOT USED
X	1	0	0	1	FORWARD RIGHT	STEER RIGHT (MOMENTARY)
X	1	0	1	0	REVERSE RIGHT	'WINCH OUT' (MOMENTARY)
X	1	0	1	1	LIGHT ON/OFF	LIGHTS ON/OFF
X	1	1	0	0	SPEED 1	SPEED 1
X	1	1	0	1	SPEED 1	SPEED 2
X	1	1	1	0	SPEED 2	SPEED 3
X	1	1	1	1	SPEED 2	SPEED 4

Table1 Decoder response to PPM codes

CIRCUIT DESCRIPTION

The decoder operates on a timescale fixed by an internal oscillator and its external timing components. The oscillator may be adjusted to a wide range of frequencies to allow different decoders to respond to different PPM rates. PPM words consist of six narrow pulses separated by 5 gaps, a short gap for a '1' and a long gap for a '0', in the ratio 2 to 3. Words are separated by a gap of ratio 6. Two complete correct adjacent words are required before the decoder will respond.

A second on-chip oscillator provides a frequency which sets the mark/space ratio of the motor speed control and hazard and indicator flasher rate. A power-on reset is also provided during initial power-up.

Simultaneous control of two independent vehicles is possible. For one vehicle the first bit of the 5-bit transmitted code is a '0' and for the second vehicle the first bit is a '1' as shown in Table 1.

OPERATING NOTES

1. In Table 1, X determines one of two vehicles to be controlled by independent controllers within the same area. The same decoder design can drive either vehicle. X = 0 for vehicle 1, X = 1 for vehicle 2.
2. Momentary controls only give an output for the duration of a PPM command stream, i.e. for as long as a transmitter button is depressed.
3. Hazard and lights control codes provide a toggle action; push once for on, push again for off. There is an internal time-out within the decoder to cater for interruptions in the PPM stream by noise.
4. Vehicle type A will drive at half or full speed and has a latching drive. The steering has three positions: hard left, centre and hard right and is driven momentarily during code transmission. The centre position may be indicated by a contact running on a conductive track attached to the steering bar (see fig.4). The track should have a non-

conducting section at the centre and the two halves should be taken to V_{SS} and V_{DD} respectively. The contact, which should be fixed to the body of the vehicle, is attached to a pin on the decoder and a two resistor bias network. The contact must not conduct with either area when in the centre position.

5. Vehicle type B also has a latched drive direction , which remains latched until STOP is pressed; but its steering is momentary, so that it will progress left (say) until the command is removed, and stay in that position until a further steering command is received. This provides a time-proportional steering system.

6. Vehicle type B has four possible drive speeds; quarter, half, three-quarters and full speed. From STOP or power-on the speed selected is quarter, or speed 1. Further speeds are selected by the four latched speed select commands. The steering speed or rate of progression is proportional to the drive speed.

7. Vehicle type B has provision for single speed driving of a third motor (forward or reverse). Control of this motor is momentary, stopping when commands cease to be transmitted.

8. One output of the decoder provides a continuous flashing signal. This can be gated with various other outputs of the decoder (using simple transistor gates) to give automatic flashing lights or buzzers when functions are operating. Examples are: left and right turn indicators, buzzer when reversing, warning lamp when winch in operation or siren switched on and off by 'lights' command.

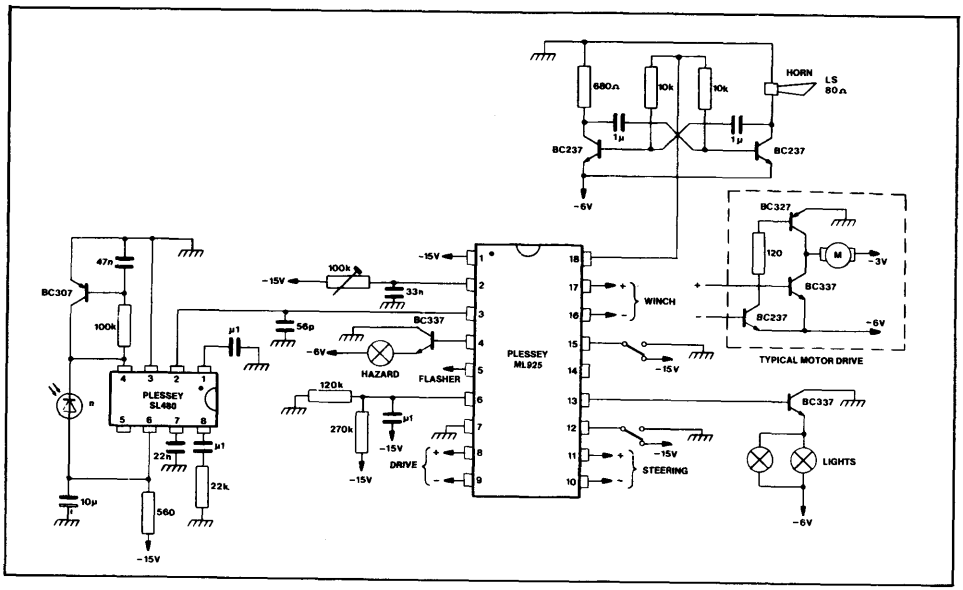

Fig.3 Infra-red control for car or truck

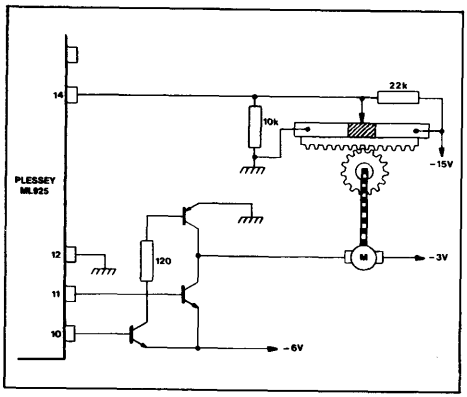

Fig.4 Infra-red control for vehicle with 3-position steering

PIN FUNCTIONS

1. **V_{DD}**
   -12V to -18V power supply.

2. **Oscillator time constant**
   An RC time constant of a capacitor to V_{SS} and a resistor to V_{DD} defines the internal clock frequency for demodulating PPM.

3. **PPM input**
   The output of the 'front end' amplifier is connected here; the signal must be a normally low level of -6V, and have PPM pulses going positive to -1V.

4. **Hazard**
   An open drain output to drive a flashing lamp or buzzer at a rate determined by pin 6 time constant. Toggled on or off by a single PPM code.

5. **Indicator signals**
   A permanently pulsing output at a rate determined by pin 6 time constant. Open drain drive.

6. **Speed time constant and power-on reset**
   A capacitor and resistor to V_{DD} and a resistor to V_{SS} define the frequency of the motor speed control pulses and the warning and indicator pulses.

7. V_{SS}
0V power supply.

8. Forward
Open drain high power latched drive to the drive motor circuit. When on, the drive motor should move the vehicle forward.

9. Reverse
Open drain high power latched drive to the drive motor circuit. When on, the drive motor should move the vehicle in reverse.

10. Steer left
Open drain high power drive to the steering motor circuit. When on, the steering should move on the left.

11. Steer right
Open drain high power drive to the steering motor circuit. When on, the steering should move to the right.

12. Vehicle type
An input to determine the type of vehicle and the interpretation of control codes. V_{SS} selects Type A (car) V_{DD} selects type B (truck).

13. Lights
Open drain output to drive headlights etc. Toggled on or off by a single PPM code.

14. Steering
An input from the centre contact of the steering feedback system for vehicle type A. A resistor to V_{SS} and a resistor to V_{DD} are required as a bias chain.

15. Code set
An input to determine which set of 16 PPM codes the decoder responds to. V_{DD} will select the first 16 (E = 0) and V_{SS} will select the last 16 (E = 1).

16. Third motor +
Open drain high power drive to a third motor circuit for vehicle type B.

17. Third motor-
Open drain high power drive to a third motor circuit for vehicle type B. Drives motor in opposite direction to pin 16.

18. Horn
Open drain output to drive a horn or buzzer. A momentary output selected by one PPM code.

Operation of the various functions is described more fully in 'operation' and in Table 1.

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ML926/7

REMOTE CONTROL RECEIVERS
(With Momentary Outputs)

The ML926 and ML927 are MOS LSI monolithic circuits for use as receivers of remote control signals for television control and many other applications. They are general purpose devices each receiving sixteen of the thirty-two codes transmitted by the SL490 circuit as pulse position modulation (PPM).

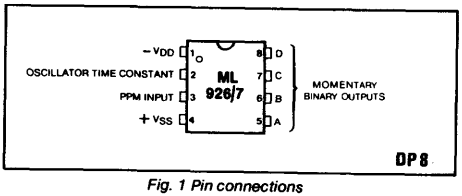

Fig. 1 Pin connections

FEATURES

- Minimum Package Size – 8-Lead Minidip
- Four Outputs Indicate in Binary the Code Currently Being Received, and Are Switched Off (Low) When No Valid Code is Detected.
- On-Chip Oscillator
- High Power, Free Drain, Output Buffers

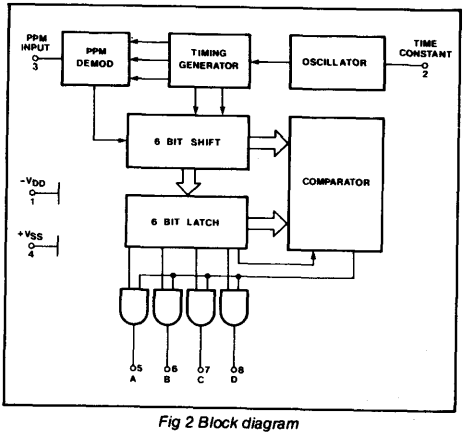

Fig 2 Block diagram

OPERATING NOTES

The receiver operates on a timescale fixed by an internal oscillator and its external timing components. The oscillator may be adjusted to any value between 15Hz and 150kHz (allowing different receivers to respond to differ – ent transmission rates within the same area).

A counter is reset whenever a pulse is received, and allowed to count at half the oscillator frequency. For example, take an oscillator frequency of 1.5kHz:–

Resetting is blocked for the first 14 ms and windows from 14ms to 22ms and from 22ms to 40ms determine whether a '1' or a '0' is present. Periods between pulses of 40ms to 80ms are recognised as word intervals. Checks are made to ensure 6 pulses, or 5 bits, are received for a word to be valid, and only after two consecutive and identical words is the receiver allowed to respond to the incoming code.

The ML926 responds only to codes 00001 to 01111 from the SL490 transmitter whereas the ML927 responds to codes 10001 to 11111.

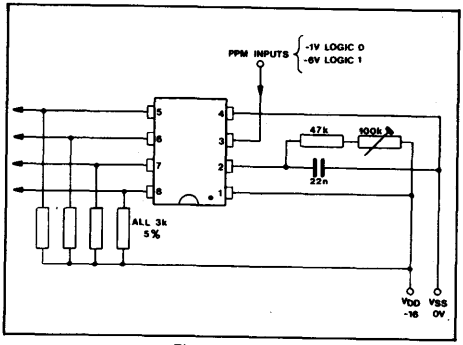

Fig. 3 Test circuit

ABSOLUTE MAXIMUM RATINGS

V_{DD} supply and inputs w.r.t. V_{SS}	+0.3V to -25V
Storage temperature	–55°C to +125°C
Operating temperature ambient	-10°C to +65°C

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
V_{DD} = −16V
T_{amb} = 25°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating supply voltage range		12	14	18	V	
Current consumption	1	2	3	4	mA	
PPM input						
Input logic level high	3	−1		O	V	
Input logic level low	3	V_{DD}		−6	V	
Input pulse width	3	1		$22T_{OSC}$	μsec	$T = \frac{1}{f_{osc}}$
Oscillator time constant See Note 1						
Oscillator frequency	2	15		150k	Hz	
			3k		Hz	Typical TC: 22nF to Vss 100k to V_{DD}
Variation wrt V_{DD}			1		%/V	
Output voltage high	5-8	-1.5		0	V	R_L = 3.0K to VDD
Output device leakage (Output OFF)	5-8			1	μA	

Note 1. R_{osc} (Pin 2) is 47kΩ → 200kΩ , $f_{osc} \simeq \frac{1}{0.15CR}$

PIN FUNCTIONS

1. V_{DD}
−14V to −18V power supply

2. Oscillator time constant
An RC time constant of a capacitor and resistor at this pin defines the internal clock frequency. The clock frequency may be varied from 15Hz to 150kHz.

3. PPM input
The output of the 'front end' amplifier is connected to this pin; the signal must consist of a normal logic 'low' level with pulses to logic 'high' corresponding to the PPM pulses from the transmitter.

4. V_{SS}
0V (ground)

5-8. A.B.C.D
Four open drain high power transistors give a binary coded output of the valid code being received.

	Momentary binary outputs	
Transmitter Code	**ML926**	**ML927**
E D C B A	**D C B A**	**D C B A**
0 0 0 0 0	0 0 0 0	0 0 0 0
0 0 0 0 1	0 0 0 1	
0 0 0 1 0	0 0 1 0	
0 0 0 1 1	0 0 1 1	
0 0 1 0 0	0 1 0 0	
0 0 1 0 1	0 1 0 1	
0 0 1 1 0	0 1 1 0	
0 0 1 1 1	0 1 1 1	
0 1 0 0 0	1 0 0 0	
0 1 0 0 1	1 0 0 1	
0 1 0 1 0	1 0 1 0	
0 1 0 1 1	1 0 1 1	
0 1 1 0 0	1 1 0 0	
0 1 1 0 1	1 1 0 1	
0 1 1 1 0	1 1 1 0	
0 1 1 1 1	1 1 1 1	
1 0 0 0 0	0 0 0 0	0 0 0 0
1 0 0 0 1		0 0 0 1
1 0 0 1 0		0 0 1 0
1 0 0 1 1		0 0 1 1
1 0 1 0 0		0 1 0 0
1 0 1 0 1		0 1 0 1
1 0 1 1 0		0 1 1 0
1 0 1 1 1		0 1 1 1
1 1 0 0 0		1 0 0 0
1 1 0 0 1		1 0 0 1
1 1 0 1 0		1 0 1 0
1 1 0 1 1		1 0 1 1
1 1 1 0 0		1 1 0 0
1 1 1 0 1		1 1 0 1
1 1 1 1 0		1 1 1 0
1 1 1 1 1		1 1 1 1

Table 1 Response to SL490 codes

PLESSEY
Semiconductors

ML928/9

REMOTE CONTROL RECEIVERS
(WITH LATCHED OUTPUTS)

Plessey Semiconductors have developed and produced a range of monolithic integrated circuits which give a wide variety of remote control facilities. As well as ultrasonic or infra-red transmission, cable, radio or telephone links may also be utilised. Pulse position modulation (PPM) is used with or without carrier and automatic error detection is also incorporated. Although initially designed with TV remote control in mind the devices may equally easily be applied for use in radios, tuners, tape and record decks, lamps and lighting, toys and models, industrial control and monitoring.

The ML928 and ML929 are general purpose remote control receivers, each receiving and latching 16 of the 32 codes transmitted by the SL490 circuit in the PPM (Pulse Position Modulation) mode. The ML928 responds to codes 00000 to 01111 only, and the ML929 to codes 10000 to 11111. Both devices are packaged in 8-lead minidip to minimise board area. The on-chip oscillator may be adjusted from 15Hz to 150kHz, allowing different transmission rates. They have a high degree of immunity to incorrect codes; there must be two consecutive correct codes received before the outputs can change.

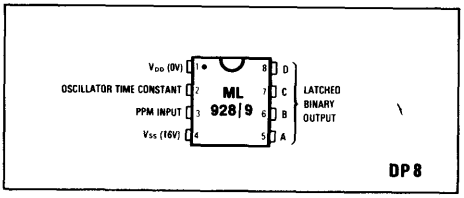

Fig. 1 Pin connections

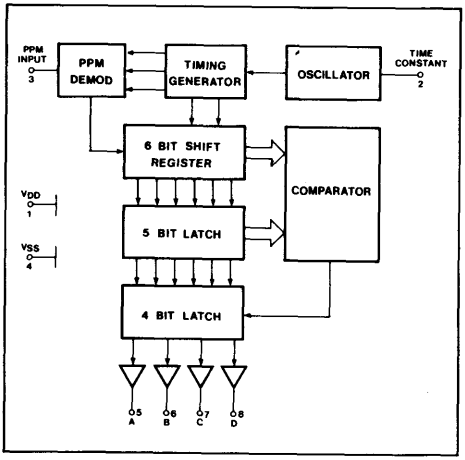

Fig. 2 ML928, ML929 remote control receivers block diagram

FEATURES

- Accepts 5 Bit PPM
- On-Chip Oscillator, 15Hz to 150kHz Range
- Easily Used With Ultrasonic, Infra-Red or Other Transmission Media
- Four High Drive Outputs
- 16 Latched States
- Minimum Sized Package

QUICK REFERENCE DATA

- Power Supply: 12V to 18V. Typical 4mA at 16V.
- Demodulation: Pulse position with time window checking by on-chip oscillator
- Decoder: 5 Bit with successive codeword comparison
- Outputs: Maximum 15mA sourced from open drain drive
- Logic convention: Logic 0 – output transistor ON, pulls output to V_{SS}
  Logic 1 – output transistor OFF

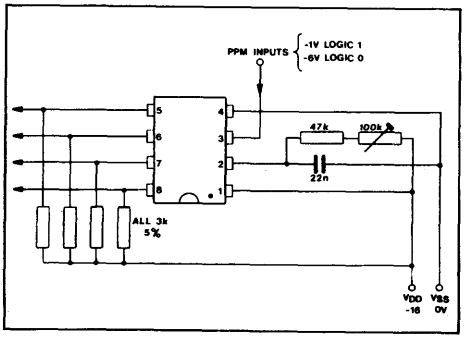

Fig. 3 Test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{SS} = 0V
V_{DD} = −16V
T_{amb} = +25°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Current Consumption V_{DD}	1	3	4	5	mA	
Supply voltage	1	−12		−18	V	
PPM input	3					
Logic '0' level		−1		0	V	
Logic '1' level		V_{DD}		−6	V	
Input pulse width		1		$22T_{osc}$	µs	$T_{osc} = \frac{1}{f_{osc}}$
Oscillator Timing	2					
Frequency		15		150k	Hz	
			4k		Hz	Typical TC: 22nF to Vss, 100kΩ to V_{DD}
Variation w.r.t. V_{DD}			1		%/V	
Latched binary output	5, 6, 7, 8	-1.5		0V	V	RL = 3.0k to VDD
Logic '0' output voltage						
Output leakage in logic '1' state				1	µA	

Note 1. $R_{osc.}$ (pin 2) is 25k → 200 kΩ. $f_{osc.} \simeq \frac{1}{0.15CR}$

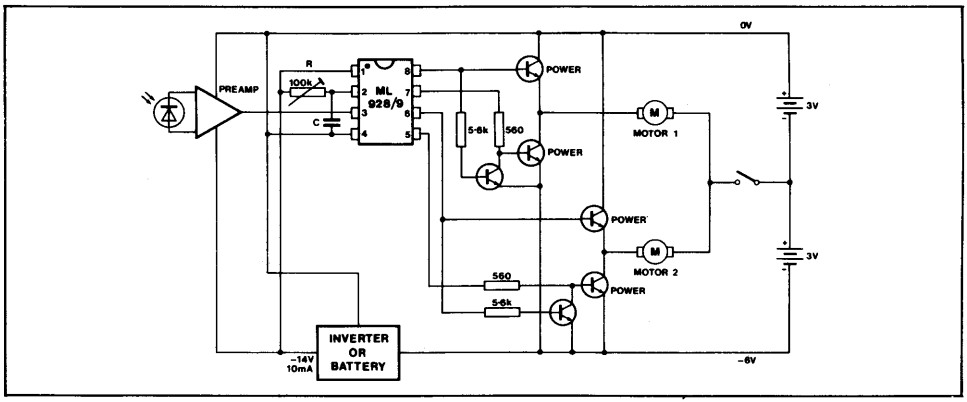

Fig. 4 Forward and reverse drive of two small DC motors

PIN FUNCTIONS

Negative logic: '0' is 0V (V_{SS}), '1' is − 12V to −18V (V_{DD})

1. V_{DD}
−12V to −18V power supply

2. Oscillator time constant
An R-C time constant at this pin defines the internal clock frequency. The clock frequency may be varied from 15Hz at 150Hz and should be set so that there are 40 periods in one 't_0' transmitter pulse interval.

3. PPM input
The output of the 'front end' amplifier is connected to this pin; the signal must consist of a normal logic '1' level with pulses to logic '0' corresponding to the PPM pulses from the transmitter.

4. V_{SS}
0V (ground)

5-8. A,B,C,D
Four open-drain high power transistors give a binary coded latched output of the last valid code received.

Transmitter Code	Latched binary outputs	
	ML928	ML929
E D C B A	D C B A	D C B A
0 0 0 0 0	0 0 0 0	
0 0 0 0 1	0 0 0 1	
0 0 0 1 0	0 0 1 0	
0 0 0 1 1	0 0 1 1	
0 0 1 0 0	0 1 0 0	
0 0 1 0 1	0 1 0 1	
0 0 1 1 0	0 1 1 0	
0 0 1 1 1	0 1 1 1	
0 1 0 0 0	1 0 0 0	No change
0 1 0 0 1	1 0 0 1	
0 1 0 1 0	1 0 1 0	
0 1 0 1 1	1 0 1 1	
0 1 1 0 0	1 1 0 0	
0 1 1 0 1	1 1 0 1	
0 1 1 1 0	1 1 1 0	
0 1 1 1 1	1 1 1 1	
1 0 0 0 0		0 0 0 0
1 0 0 0 1		0 0 0 1
1 0 0 1 0		0 0 1 0
1 0 0 1 1		0 0 1 1
1 0 1 0 0		0 1 0 0
1 0 1 0 1		0 1 0 1
1 0 1 1 0	No change	0 1 1 0
1 0 1 1 1		0 1 1 1
1 1 0 0 0		1 0 0 0
1 1 0 0 1		1 0 0 1
1 1 0 1 0		1 0 1 0
1 1 0 1 1		1 0 1 1
1 1 1 0 0		1 1 0 0
1 1 1 0 1		1 1 0 1
1 1 1 1 0		1 1 1 0
1 1 1 1 1		1 1 1 1

Table 1 Response to SL490 codes

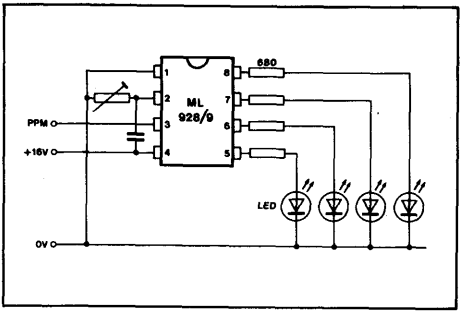

Fig. 5 Direct drive of LEDs

ABSOLUTE MAXIMUM RATINGS

V_{DD} supply and inputs w.r.t. V_{SS}	+0.3V to −25V
Storage temperature	−55°C to +125°C
Operating temperature ambient	−10°C to +65°C

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SL470

BCD TO 1 OF 10 DECODER/VARICAP DRIVER

FEATURES

- Up To 10 Programmes
- Direct Varicap Voltage Selection
- TTL Level Compatible Inputs
- May be Directly Driven by ML920 Series Receivers
- Low Component Count
- Low Cost
- Can Be Used To Drive Indicators

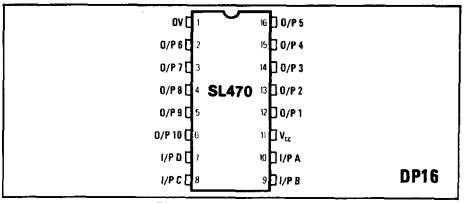

Fig. 1 Pin connections

QUICK REFERENCE DATA

- Power supply 33V 3mA
- 1 out of 10 outputs selected high
- Output drive 2mA
- Input 4 Bit BCD, TTL compatible

D(2^3)	C(2^2)	B(2^1)	A(2^0)	O/P (high)
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10

Table 1 Decode table

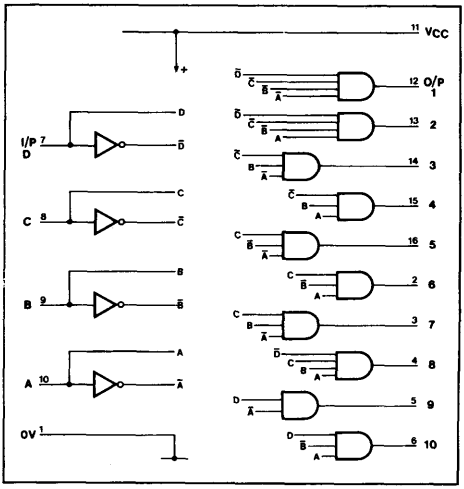

Fig. 2 Logic diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = 25°C$
$V_{CC} = 33V$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating supply voltage	11	30		36	V	
Supply current	11		2	3	mA	O/Ps unloaded
Selected output level	2–6, 12–16		V_{CC} - 1.5	Vcc–3.5	V	I_{OUT} = 2mA
Unselected output levels	2–6, 12–16	0.5			V	100k load to 0V
Input high state	7–10	1.7		5	V	
Input low state	7–10	–0.3		+0.4	V	
Input current	7–10			1.5	mA	V_{in} = 1.7V

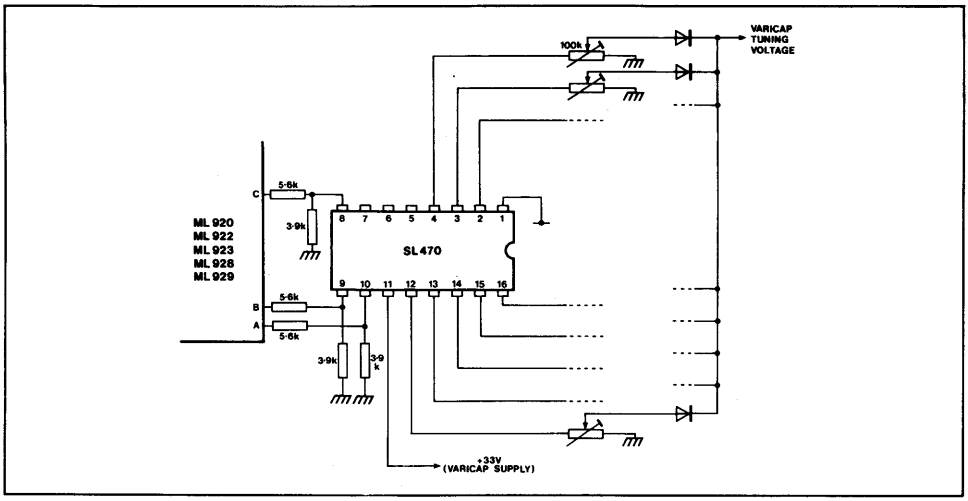

Fig.3 Typical application circuit for 8 programmes

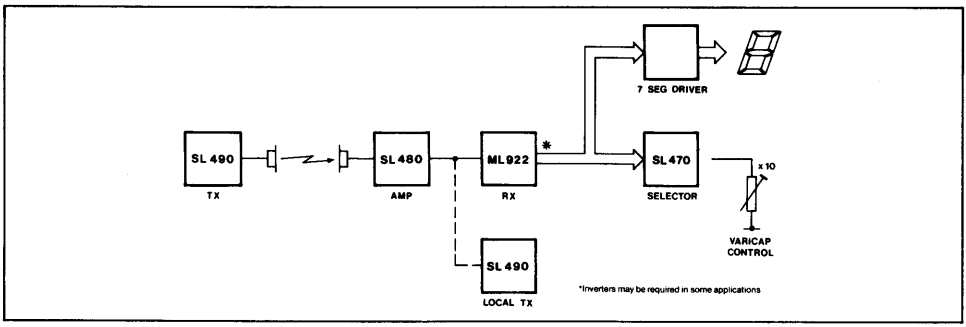

Fig. 4 Complete remote control system

ABSOLUTE MAXIMUM RATINGS

Storage temperature	—55°C to +125°C
Operating temperature	—10°C to +65°C
Supply voltage	36V

PLESSEY
Semiconductors

SL480

INFRA-RED PULSE PRE-AMPLIFIER

The SL480 is a bipolar integrated circuit containing three amplifier stages. Its output is directly compatible with the ML920 range of remote control receiver circuits. It is packaged in an 8-lead plastic package. The gain of the amplifier stages may be adjusted to suit the application. The input impedance is approximately 20MΩ.

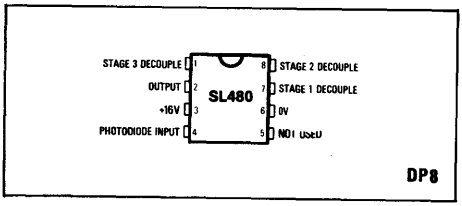

Fig. 1 Pin connections

FEATURES

- Minimum Component Solution to Infra-Red Detection
- Adjustable Gain
- Directly Compatible With Plessey ML920 Range of Receivers
- May Be Used As A General Purpose 100kHz Limiting Amplifier

ABSOLUTE MAXIMUM RATINGS

Supply, Vcc	20V
Maximum power dissipation	480mW
Operating temperature range	−10°C to +65°C
Storage temperature range	−55°C to +125°C

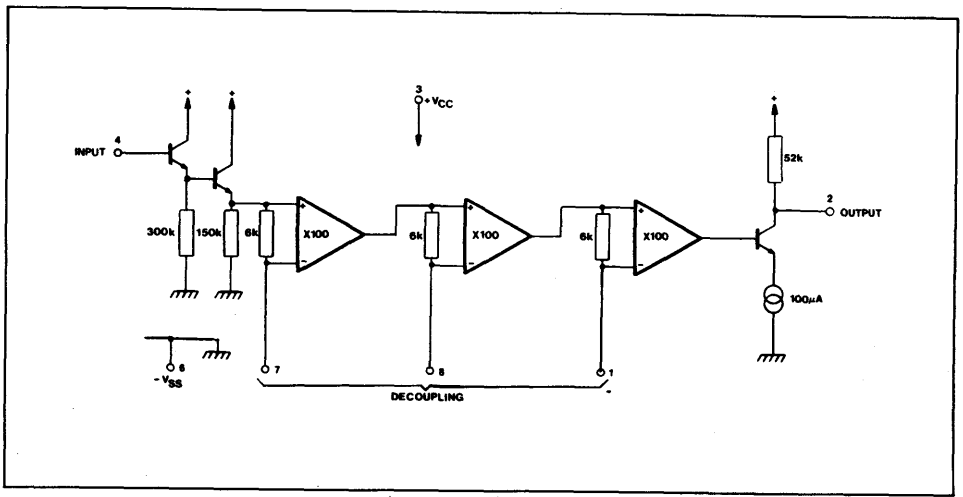

Fig. 2 SL480 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C
V_{CC} = +15V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range	3	12		18	V	
Supply current	3		1.5	4	mA	
Open loop gain	4, 2		100		dB	Sum of 3 stage gains
Input impedance	4		20		MΩ	
Output current sink	2		100		μA	
Internal pullup resistor	2		50		kΩ	
Quiescent O/P voltage (low)	2	9	11		V	At reduced gain
Pulse output (high)	2	15.5			V	No load

OPERATING NOTES

An external resistor of, typically, 330kΩ between pins 4 and 3 provides current for the photo detector diode connected across pins 4 and 6. Any voltage generated across the diode by incident light is amplified.

The gain of each stage may be readily adjusted by external resistors in series with decoupling capacitors between pins 7, 8 or 1 and ground. For maximum gain the resistors are dispensed with except at pin 8.

Typical decoupling capacitors are 22nF. The output goes high towards Vcc when light is detected. This is compatible with the PPM input of the ML920 series of remote control receivers. The SL480 is compatible with the full power supply range of the ML920 series and can also be used at a lower supply voltage as long as Vcc is common to Vss of the MOS device, i.e. common positive.

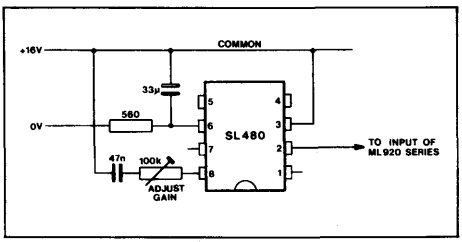

Fig.3 Gain adjustment, common positive

The circuit diagram of the SL480 infra-red pulse amplifier is shown in Fig.5. Pulses generated by an infra-red receiver diode are amplified to a suitable level for direct connection to the input of any of the Plessey Semiconductors ML900 series of remote control receiver circuits.

For basic operation, the receiving diode and SL480 input is biased with a single resistor to the positive supply. Any infra-red light reaching the diode generates a leakage current which causes a voltage drop across the bias resistor.

The SL480 input stage consists of a compound emitter follower (TR1 and TR2) which provides a high input impedance and allows a relatively high diode load resistor as well as a voltage drop of around 1.3V between the input and the bases of the first amplifier stage (TR6, TR7).

Transistors TR6 and TR7 form a differential amplifier which is designed to prevent low frequency or DC input signals from reaching subsequent stages of the amplifier. Since the bases of transistors TR6 and TR7 are internally connected by the 6.3k resistor R3, low frequency signals are applied to both sides simultaneously causing no change in collector current and therefore no output to the second stage. Higher frequency signals are amplified because TR7 base is decoupled externally on pin 7.

Stage 2 gain is provided by a similar differential amplifier to stage 1 except that the relatively stable DC input voltage provided by stage 1 output allows the use of a tail resistor R11 rather than a current source. Decoupling of AC signals is provided at pin 8.

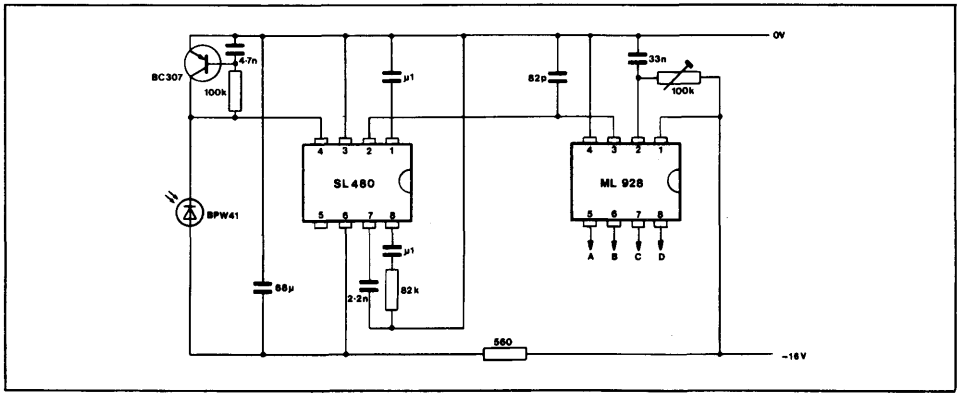

Fig.4 Compact infra-red receiver

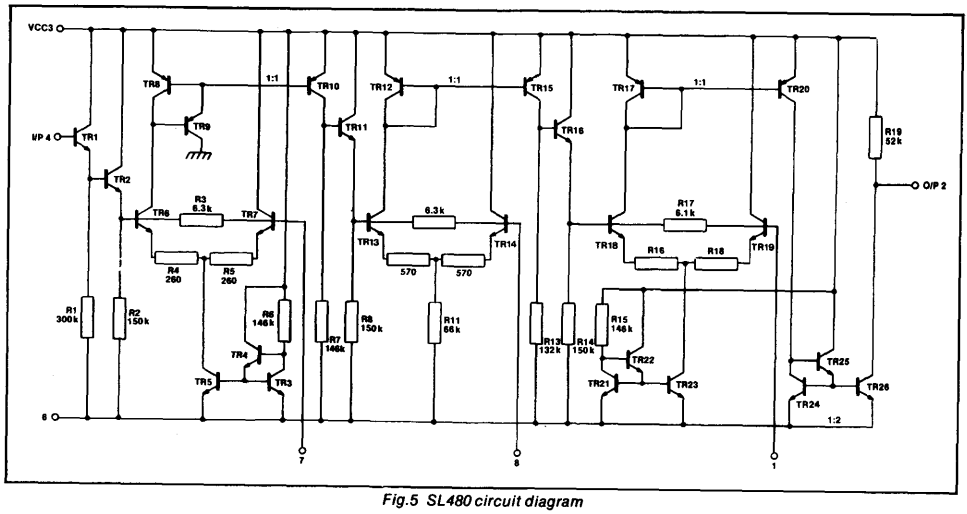

Fig.5 SL480 circuit diagram

Stage 3 is similar to stage 1, but with an extra current mirror (TR24 to TR26) to provide signal inversion at the output.

The standing current through the output load resistor and thus the output voltage, is set by the current in R15. This current will amount to about 100μA, and give an output voltage about 5V below the positive rail with a 15V supply.

It should be noted that there is a parasitic zener diode of about 6V in parallel with the output load resistor R19; this diode will be destroyed if the output is shorted to the negative supply rail. Stage 3 decoupling is provided at pin 1.

With a 15V supply, the input stage will operate with input voltages ranging from 15V down to 5V. This will allow the device to function satisfactorily in high ambient light conditions which produce high leakage currents in the receiving diode. A single transistor circuit is shown in Fig.6, which prevents the input voltage to the SL480 changing for diode leakage currents up to several milliamps. By careful choice of R and C values, this circuit can be made to give extra rejection of low frequency modulation such as that produced by incandescent lamps.

Under conditions of very high ambient light the circuit may show signs of instability. This can be prevented by connecting a 2.2k resistor in series with the transistor emitter.

If required, the gain of each stage of the SL480 can be set individually by connecting a resistor in series with the decoupling capacitor. A 6k resistor will reduce the stage gain to half its full value of about 40dB. Normally it is only necessary to reduce the gain of the second stage with about 33-56k.

If preferred the decoupling components on pins 1, 7 and 8 can be earthed to the negative supply on pin 6.

As with any high gain device, care is needed in the layout of printed circuit boards to prevent instability. All decoupling and input components should be mounted close to the SL480. A suitable printed circuit layout for the SL480 is shown below.

Decoupling of the power supplies local to the SL480 is advisable. A resistor of about 560ohms in series with the negative rail and a parallel capacitor of 68microfarads being adequate (see Fig.6).

The decoupling resistor should always be in the negative supply as the ML920 series remote control circuits have a threshold close to the positive rail, and any voltage drop here would reduce the noise immunity.

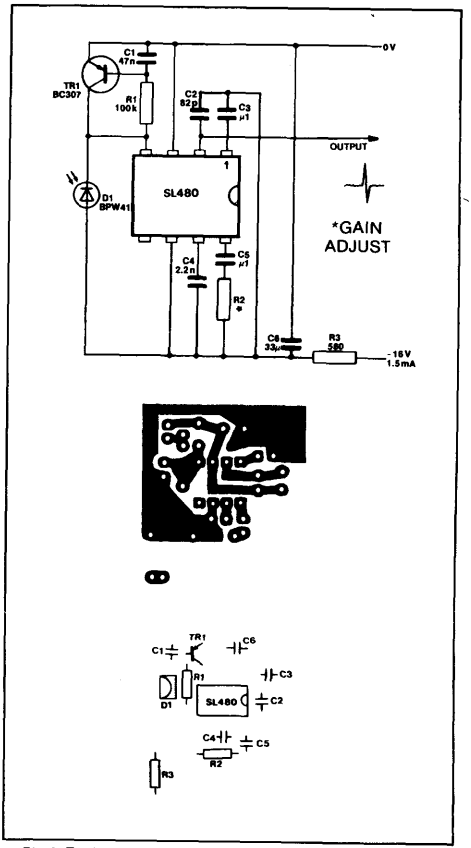

Fig.6 Typical infra-red amplifier application with improved detector biasing

PLESSEY
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SL490

REMOTE CONTROL TRANSMITTER

Plessey Semiconductors have developed and produced a range of monolithic integrated circuits which give a wide variety of remote control facilities. As well as ultrasonic or infra red transmission, cable, radio or telephone links may also be utilised. Pulse position modulation (PPM) is used with or without carrier and automatic error detection is also incorporated. Although initially designed with TV remote control in mind the devices may equally easily be applied for use in radios, tuners, tape and record decks, lamps and lighting, toys and models, industrial control and monitoring.

The SL490 is an easily extendable, 32 command, pulse position modulation transmitter drawing negligible standby current. It may be used with the ML920 series of remote control receivers.

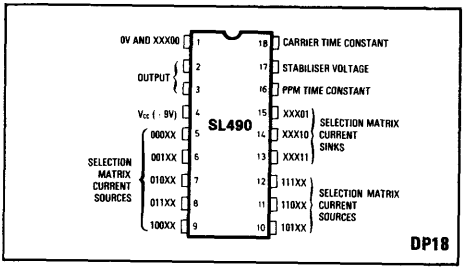

Fig. 1 Pin connections

FEATURES

- Ultrasonic or Infra-red Transmission
- Direct Drive for Ultransonic Transducer
- Direct Drive of Visible LED When Using Infra-red
- Very Low Power Requirements
- Pulse Position Modulation Gives Excellent Immunity From Noise and Multipath Reflections
- Single Pole Key Matrix
- Switch Resistance Up To 1kΩ Tolerated
- Few External Components
- Anti-Bounce Circuitry On Chip

QUICK REFERENCE DATA

- Power Supply: 9V, Standby 6μA, Operating 8mA
- Modulation: Pulse Position With or Without Carrier
- Coding: 5 Bit Word Giving a Primary Command Set of 32 Commands
- Key Entry: 8 × 4 Single Pole Key Matrix
- Data Rate: Selectable 1 Bit/Sec to 10k Bit/Sec.
- Carrier Frequency: Selectable 0Hz (no carrier) to 200kHz.

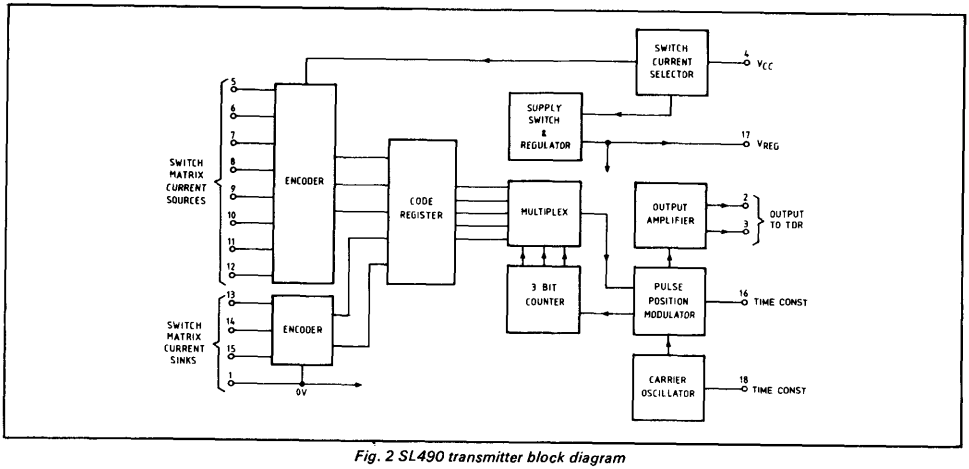

Fig. 2 SL490 transmitter block diagram

ELECTRICAL CHARACTERISTICS (see Fig.3)

Test conditions (unless otherwise stated):
T_{amb} = 25°C fc = 40kHz
Vcc = +7V to + 9.5V t_1 = 18ms

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating supply current	4		8	16	mA	Vcc = 9.5V
Standby supply current	4			30	µA	
Stablised voltage	17	4.3	4.6	4.9	V	
Output current available	17			1	mA	
Output voltage swing	2, 3	1		Vcc	V	Unloaded
Output current	2, 3			5	mA	Peak value
External switch resistance				1	kΩ	
External switch closure time		6			ms	
External carrier oscillator resistor required, R2	18	20	40	80	kΩ	C2 = 680pF
External PPM resistor R_1 required	16	15	30	60	kΩ	C1 = 0.68µF
Ratio to/t_1	2, 3	1.4	1.5	1.6		
Pulse width, t_p	2, 3	2	3	4	ms	
Inter word gap, t_g	2, 3	50	54	58	ms	
Variation of t_o with V_{CC} t_o with V_{CC} = 9.5V t_o with V_{CC} = 7.5V	2,3	0.96		1.04		
Pulse width T_p	2,3	2	3	4	ms	
Inter word gap t_g	2,3	50	54	58	ms	

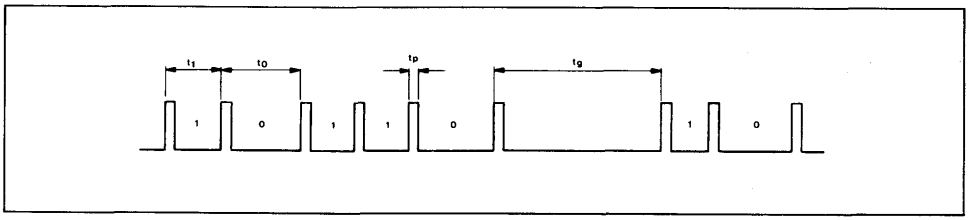

Fig.3 PPM word notation

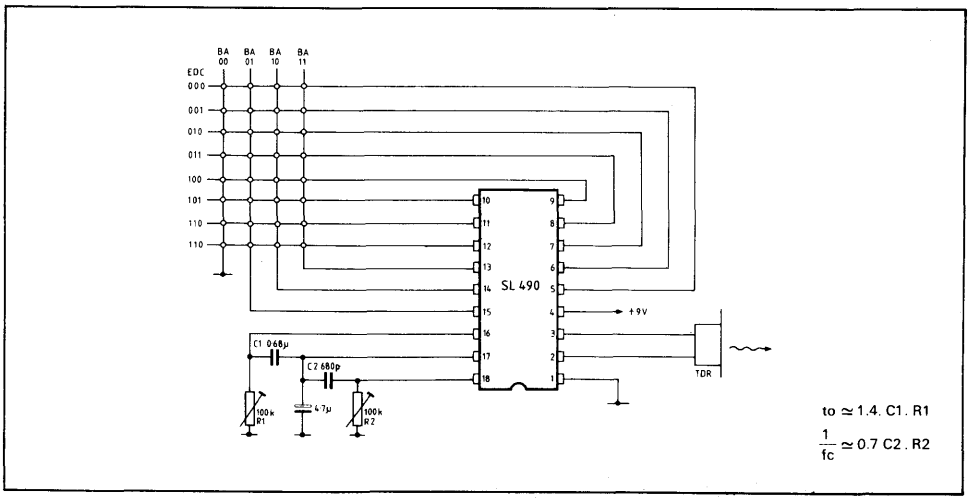

Fig. 4 Test and ultrasonic application circuit

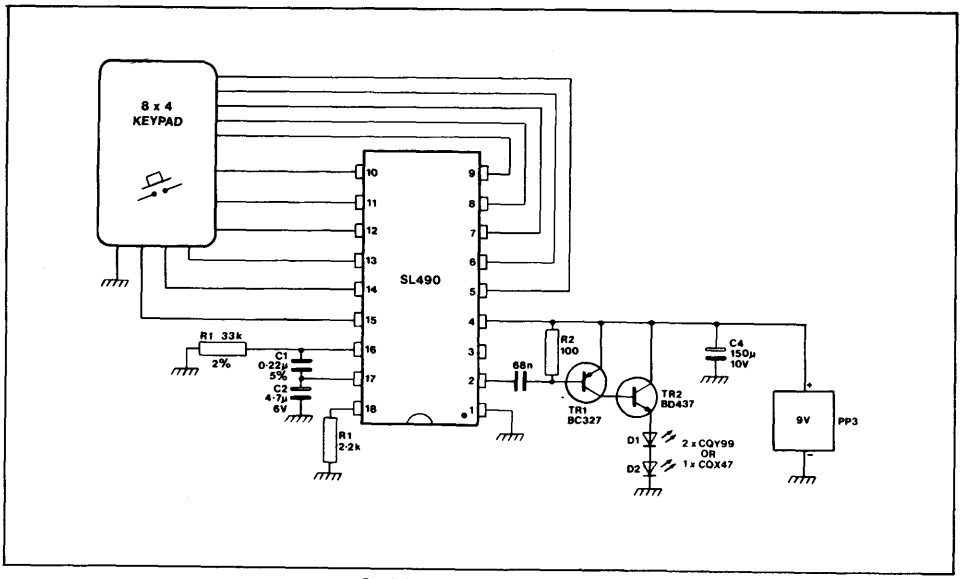

Fig.5 Infra-red application circuit

OPERATING NOTES

Fig.5 shows the circuit for a simple infra-red transmitter where the PPM output from pin 2 of the SL490 is fed to the base of the PNP transmitter TR1, producing an amplified current pulse about 15μsec wide. This pulse is further amplified by TR2 and applied to the infra-red diodes D1 and D2.

The current in the diodes and the infra-red output is controlled by the quantity, type, and connection method of the diodes and also by the gain at high currents of the transistors.

The most common solution where cost is important is to use 2 single-chip diodes, such as the CQY99 connected in series.

Improved output can be obtained by using four CQY99 diodes in a series parallel arrangement, but it is usually simpler to use 2 multichip diodes such as the CQX47 connected in parallel or a single CQX19 which gives similar results.

A significant increase in range can be obtained by using diodes such as the CQY99 in conjunction with a plated plastic parabolic reflector.

When building the transmitter, care should be taken with the choice of the capacitor C2 and with the circuit layout, particularly when multi-chip diodes are being used, as the current pulses can be as high as 6 to 8Amps.

Transistor choice is also important and any substitutes should have high current gain characteristics and switching speeds similar to those specified in Fig.3.

An increase in output can be obtained by connecting TR2 in common emitter configuration, but care should be taken not to exceed the rating of the diodes.

Choice of PPM Frequencies

Although the ML920 series of remote control receivers is designed to work over a wide range of PPM frequencies, the actual usable range may be restricted by the application. The analogue outputs on the ML920, ML922 and ML923 serve as a good example, since the outputs will step up or down, one step for each pair of PPM words received. This in turn fixes the rate of increment or decrement of the volume or colour controls of a TV set.

When the transmitter is being used with an infra-red link, with high current pulses fed to the diodes as in Fig.5, power consumption will increase with frequency. It is thus advisable that with a battery power supply, the slowest PPM rate consistent with adequate response time should be chosen.

Setting Up Procedure

When designing a system using the SL490/491 transmitters and the ML920 series receivers, it is not necessary to adjust the PPM rate on both transmitter and receiver. The usual arrangement is to have a fixed resistor of 33k from pin 16 of the SL490/491 and to choose the capacitor connected for pin 16 to pin 17 to give the required PPM rate. The value is calculated from the formula $t_o = 1.4CR$. Provided fairly close tolerance components are used for C1 and R1, then assembled transmitter units should be interchangeable without adjustment.

The timing components on the receiver can be selected using the formula

$$f_{rx} = \frac{1}{0.15CR} \text{ where } f_{rx} = \frac{40}{t_o}$$

t_o being the PPM logic 0 time from the transmitter.

The value of R for the receiver should be between 47k and 200k, a typical arrangement being to use a 47k fixed resistor and a 100k pot as shown in Fig.6. The capacitor should be selected from the above formula to give the nominal frequency somewhere near the mid-range setting of the potentiometer.

Final adjustment is made by setting the period on the receiver oscillator time constant pin to 1/40th of the transmitter PPM logic 0 time using the potentiometer. Connection to the receiver time constant pin should be made using a x10 oscilloscope probe to reduce circuit loading.

When adjusting the ML920, the monitor output can be used for setting up, but in this case, a figure of 1/20th of the transmitter PPM logic 0 time should be used as the monitor output is at half the oscillator frequency.

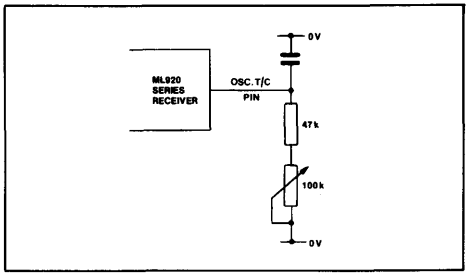

Fig.6 Recommended receiver time constant components

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7V to 9.5V
Total power dissipation	600mW
Operating temperature range	–10°C to +65°C
Storage temperature range	–55°C to +125°C

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ADVANCE INFORMATION

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SL491

REMOTE CONTROL TRANSMITTER

Plessey Semiconductors have developed and produced a range of monolithic integrated circuits which give a wide variety of remote control facilities. As well as ultrasonic or infra red transmission, cable, radio or telephone links may also be utilised. Pulse position modulation (PPM) is used with or without carrier and automatic error detection is also incorporated. Although initially designed with TV remote control in mind the devices may equally easily be applied for use in radios, tuners, tape and record decks, lamps and lighting, toys and models, industrial control and monitoring.

The SL491 is an easily extendable, 32 command, pulse position modulation transmitter drawing negligible standby current. It may be used with any ML920 series remote control receivers. The carrier oscillator may gate the PPM at a slow rate, producing bursts of transmission.

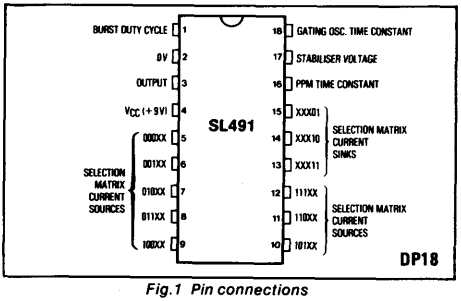

Fig.1 Pin connections

FEATURES

- Ultrasonic or Infra-red Transmission
- Multi-Transmitter Burst Mode Facility
- Burst Duty Cycle Variable
- Very Low Power Requirements
- Pulse Position Modulation Gives Excellent Immunity From Noise and Multipath Reflections
- Single Pole Key Matrix
- Switch Resistance Up To 1kΩ Tolerated
- Few External Components
- Anti-Bounce Circuitry On Chip

QUICK REFERENCE DATA

- Power Supply: 9V, Standby 6μA, Operating 8mA
- PPM with or without Carrier or Burst Mode
- Coding: 5 Bit Word Giving a Primary Command Set of 32 Commands
- Key Entry: 8 × 4 Single Pole Key Matrix
- Data Rate: Selectable 1 Bit/Sec to 10k Bit/Sec.
- Carrier Frequency: Selectable 0Hz (no carrier) to 200kHz.

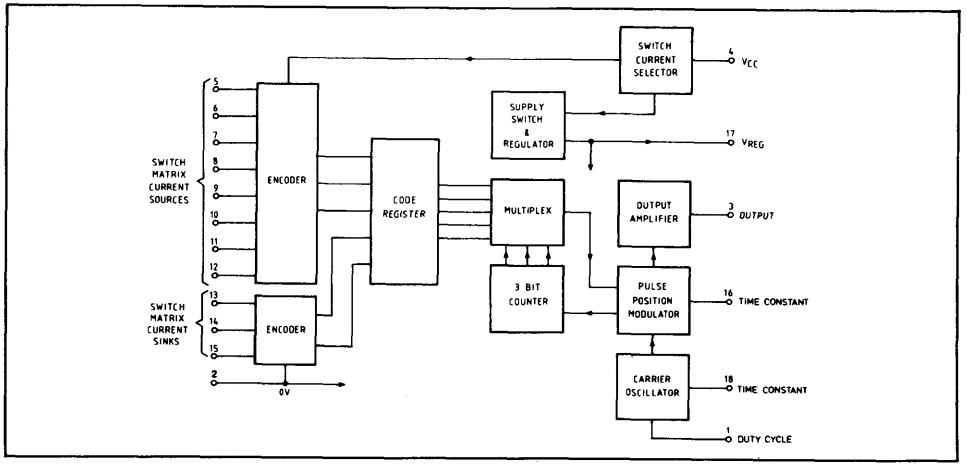

Fig.2 SL491 transmitter block diagram

ELECTRICAL CHARACTERISTICS (see Fig.4)

Test conditions (unless otherwise stated):
$T_{amb} = 25°C$ $t_0 = 9ms$
$V_{CC} = 9V$ $t_1 = 6ms$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating supply current	4		8	16	mA	$V_{CC} = 9.5V$
Standby supply current	4			30	μA	
Stabilised voltage	17	4.3	4.6	4.9	V	No external load
Output current available	17			1	mA	
Output voltage, V_0, low	3			1.6	V	50mA sink
Output current	3			100	mA	Peak value
External switch resistance				1	kΩ	
External switch closure time		30			ms	
Gating oscillator frequency			8		Hz	C2 = 1μF, R = 30kΩ
Resistor R2 for carrier frequency = 40kHz	18	10		50	kΩ	C2 = 1nF
External PPM resistor R1 required	16	15	30	60	kΩ	C1 = 220nF
Ratio t_0/t_1	2, 3		1.5			
Pulse width, t_p	2, 3		1		ms	
Inter word gap, t_g	2, 3		18		ms	

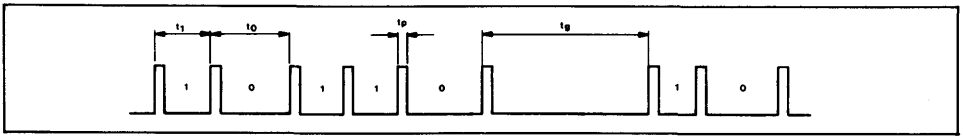

Fig.3 PPM Word Notation

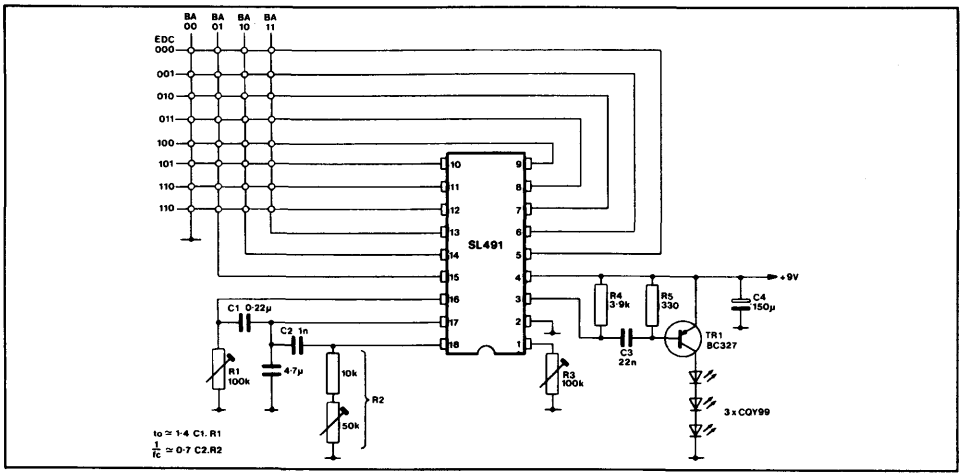

Fig.4 Test circuit and low power application

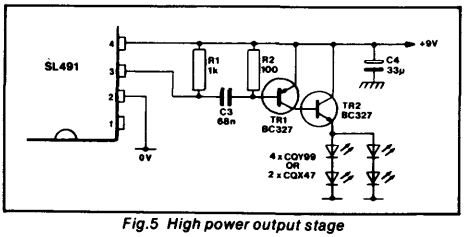

Fig.5 High power output stage

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7V to 9.5V
Total power dissipation	600mW
Operating temperature range	−10°C to +65°C
Storage temperature range	−55°C to +125°C

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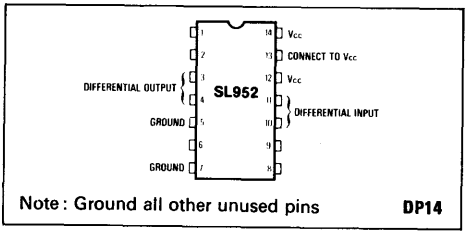
SL 952

UHF PRESCALER AMPLIFIER

The SL952 amplifier has been designed to drive the prescaler (SP4020, CT1110 etc) in a frequency synthesis system directly from the tuner's local oscillator.

It features a differential output to reduce local oscillator radiation, and a differential input, which may be used to couple the outputs from a VHF and a UHF tuner (see Fig. 3).

The device operates from a single 5V supply with a minimal number of external components and is encapsulated in a 14 lead DIL package.



Note: Ground all other unused pins **DP14**

Fig. 1 Pin connections

FEATURES

- Low Cost
- High Gain
- Minimal External Component Count
- Good Limiting Characteristics
- 1GHz Response
- 5V Supply

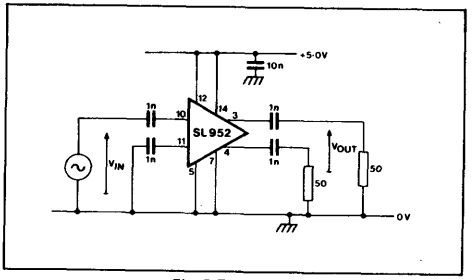


Fig. 2 Test circuit

ABSOLUTE MAXIMUM RATINGS

Vcc +10V
Ambient temperature 0°C to +65°C
Storage temperature −55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Vcc = 5.0V
TAMB = +25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply voltage	4.75	5.00	5.50	V	
Supply current		70	90	mA	
DC output level		3.2		V	
Output offset		100	600	mV	
Maximum differential output swing	600			mVp−p	
Differential voltage gain	30	35		dB	950MHz
Differential voltage gain	30	35		dB	100MHz
Differential voltage gain	15	26		dB	500MHz
					950MHz

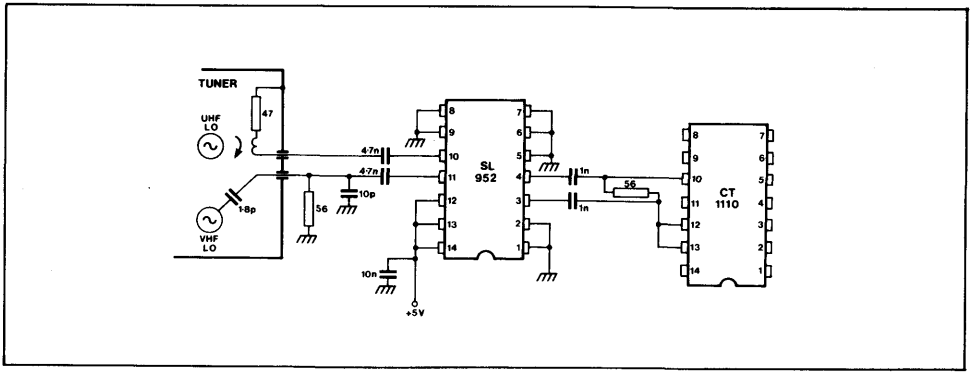


Fig. 3 Typical application for TV frequency synthesis

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SL955

UHF PREAMPLIFIER

The SL955 amplifier is a general purpose device for use at frequencies up to 1GHz. It features a differential input and output, and good linearity. The device operates from a single 5V supply with a minimal number of external components and is encapsulated in an 8-lead DIL package (DP8).

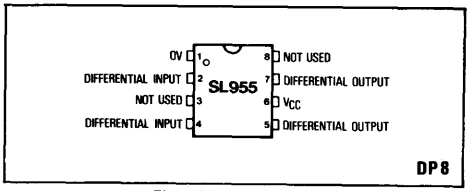


Fig.1 Pin connections

FEATURES

- Low Cost
- 22dB Gain (S_{21})
- Minimal External Component Count
- Good Linearity
- Differential Input and Output
- 1GHz Response
- 5V Supply

ABSOLUTE MAXIMUM RATINGS

V_{CC} + 10V (short term)
Operating temperature -10°C to +65°C
Storage temperature -55°C to +125°C

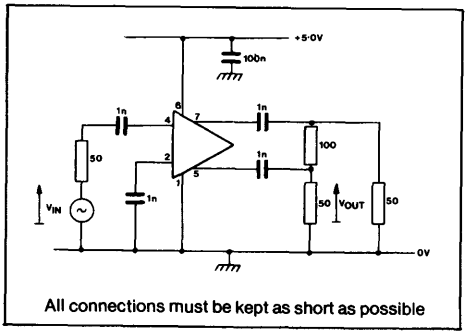


Fig.2 Test circuit

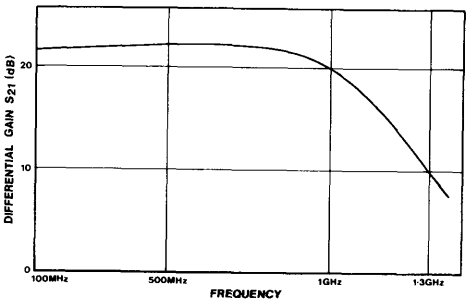


Fig.3 Typical frequency response

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = 5.0V, T_{amb} = 25°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	6	4.75	5.0	5.5	V	
Supply current	6	30	50	70	mA	
Differential gain S_{21}		16	22		dB	10 to 900MHz
Differential gain S_{21}			20		dB	1GHz
Differential gain S_{21}			10		dB	1.3GHz
Input signal handling	2, 4		25		mV rms	-40dB intermodulation
Noise figure			12		dB	

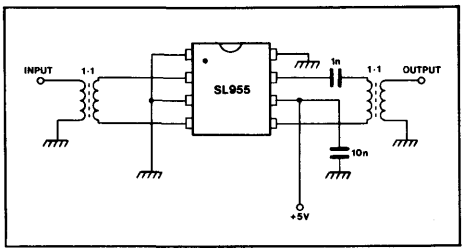


Fig.4 Typical application

PLESSEY
Semiconductors

SL 1430

TV IF PREAMPLIFIER

The SL1430 is a fixed gain IF preamplifier for television with an output optimised for driving Plessey second generation low capacitance surface acoustic wave (SAW) filters. The addition of one external capacitor allows the amplifier to drive normal capacitance SAW filters from Plessey or from other manufacturers.

The device features on chip decoupling and differential output, requiring a minimal number of external components to be used.

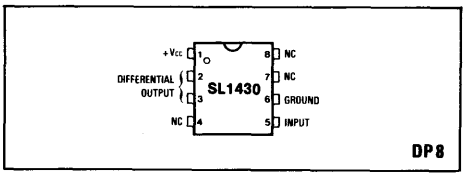


Fig. 1 Pin connections (top view)

FEATURES

- Low cost
- Low noise
- Low external component count
- Low distortion
- Direct 12V operation
- Can be used with different types of SAW filters

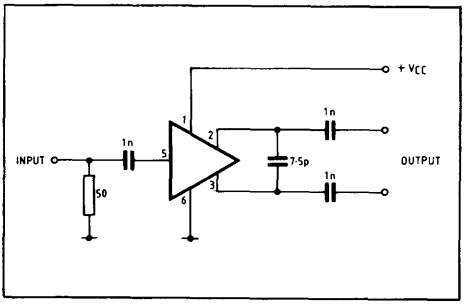


Fig. 2 Test circuit

QUICK REFERENCE DATA

- 22dB gain at 40MHz
- 12V supply at 25mA
- 120mV rms. input handling

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C
Supply voltage = +12V
Frequency = 40MHz
Output load = 7.5 pF (Pins 2 and 3)
Measurements made using test circuit Fig. 2.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply voltage	1	7	12	13.5	V	
Quiescent current	1	22	33	40	mA	Pins 2, 3O/C
Cut-off frequency (−3dB)	5, 2/3	60	110		MHz	
Voltage gain		18	22	26	dB	
Imput signal for 46dB intermodulation	5		120		mV	Red colour bar
Input signal for 1% crossmodulation	5		75		mV	(wanted level 20mV unwanted modulation 65%)
Input signal for 1dB sync tip compression	5	130			mV	rms.
Input impedance	5		300Ω// 4.2pF			

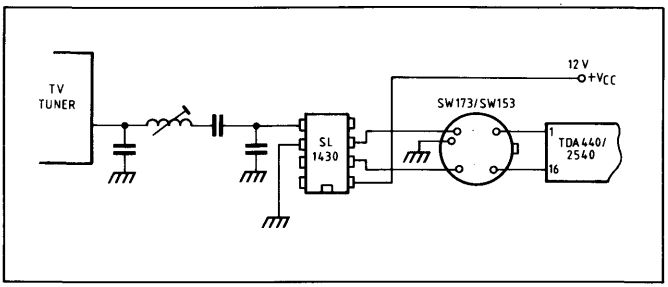


Fig. 3 Typical applications

SL1430 TYPICAL CHARACTERISTICS AT ,12V, +25°C, WITH SW173 AS LOAD (7.5pF) (FIGS. 5 TO 10) Unwanted signal with 65% amplitude modulation at 10KHz

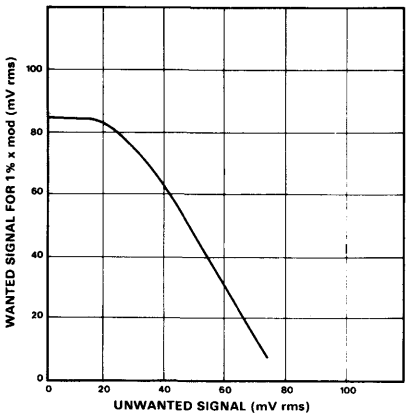


Fig. 4 Cross modulation performance (see note 1)

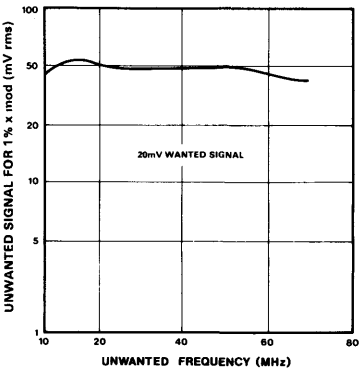


Fig. 6 Cross modulation performance V frequency of unwanted signal (see note 1)

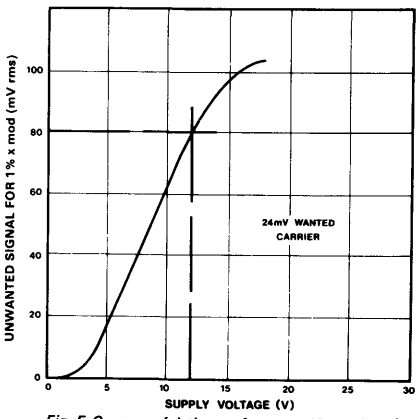


Fig. 5 Cross modulation performance V supply voltage (see note 1)

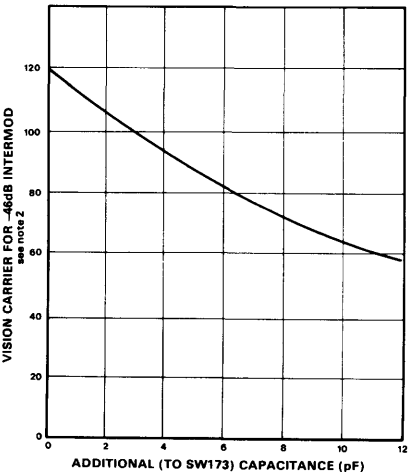


Fig. 7 Intermodulation performance v. load capacitance

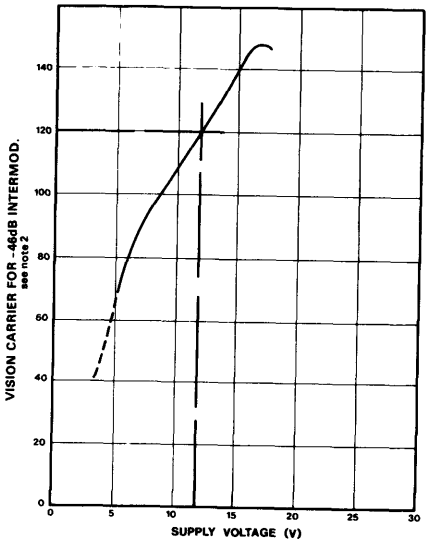


Fig. 8 Intermodulation performance v. supply voltage

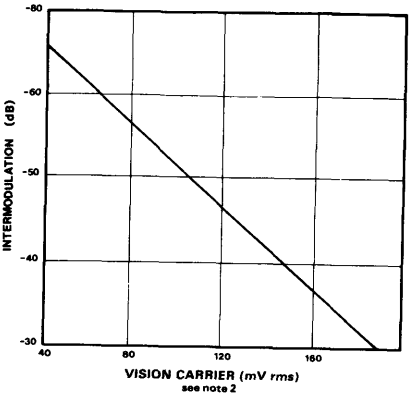


Fig. 9 Intermodulation performance (see note 2)

NOTE 1. Signal level refers to peak rms. i.e. The effective sync. tip level of a composite video signal.

NOTE 2. The test signal employed corresponds to the red bar of a transmitted colour bar and consists of the following elements related to the sync. tip level, the vision carrier at 38.9MHz–6dB, the colour carrier at 34.5MHz–18dB, and the sound carrier at 33.4MHz–7dB.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	—0.5V to +25V
Operating temperature range	—10°C to +65°C
Storage temperature range	—55°C to +125°C

PLESSEY
Semiconductors

SL 1431/2

TV IF PREAMPLIFIERS WITH AGC GENERATOR

The SL1431 and SL1432 are fixed gain IF preamplifiers for television with a differential output optimised for driving Plessey surface acoustic wave (SAW) filters. Besides providing the necessary gain block between the tuner and SAW filter they also supply a properly derived, broadband AGC signal to the tuner, the SL1431 providing the correct sense signal for a NPN tuner, and the SL1432 for an PNP tuner. The tuner AGC threshold is internally preset to a value to allow adequate signal handling in the SL1431 and SL1432 and does not normally require any external adjustment. However, to account for the large variations in signal handling capability which is encountered on some tuners, the tuner AGC threshold may be externally adjusted by altering the bias on pin 1.

Both devices feature on-chip decoupling for a minimum external component count.

AGC Signal

For high input signal levels the voltage on pin 7 goes low with SL1431 and high with the SL1432.

QUICK REFERENCE DATA

- 23dB Gain at 40MHz
- 12V Supply at 25mA
- 120mV R.M.S. Input Handling
- 15mA Tuner AGC Capability

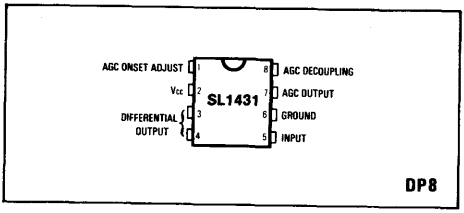


Fig. 1 Pin connections

FEATURES

- Properly Derived Tuner AGC
- Low Cost
- Low Noise
- Low External Component Count
- Low Distortion
- Direct 12V Operation
- Can be used with Different Types of SAW Filters

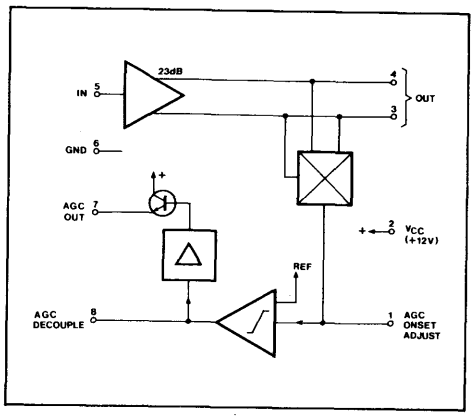


Fig. 2 Block diagram

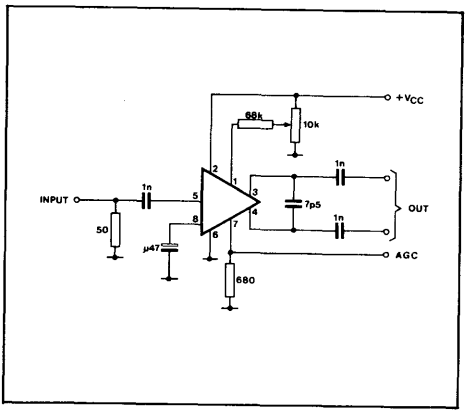


Fig. 3 Test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C
Supply voltage = +12V
Frequency = 40MHz
Output load = 7.5pF (Pins 3 and 4)
Measurements made using test circuit Fig. 3.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply Voltage	2	7	12	13.5	V	
Quiescent Current	2	22	33	40	mA	Pins o/c
Cut-off frequency (—3dB)	5	60	110		MHz	
Voltage gain		20	23	26	dB	
Input signal for 46dB intermodulation	5		120		mV	Red colour bar
Input signal for 1% cross-modulation	5		75		mV	(wanted level 20mV, unwanted modulation 65%)
Input signal for 1dB sync tip compression	5	130			mVrms	
Input impedance	5		300Ω //4.2pF			
Tuner AGC						
Output current	7	15	20		mA	@ 10.0 V
Input impedance	1		6		kΩ	

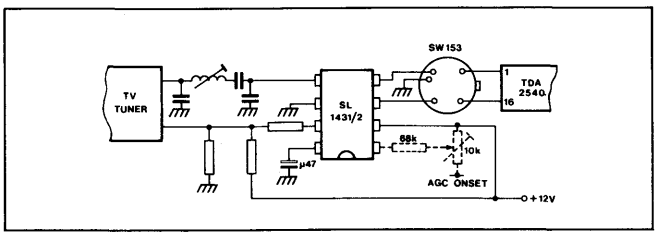


Fig. 4 Typical applications

SL1431 TYPICAL CHARACTERISTICS AT ,12V, +25°C, WITH SW173 AS LOAD (7.5pF) (FIGS. 5 TO 10) Unwanted signal with 65% amplitude modulation at 10kHz

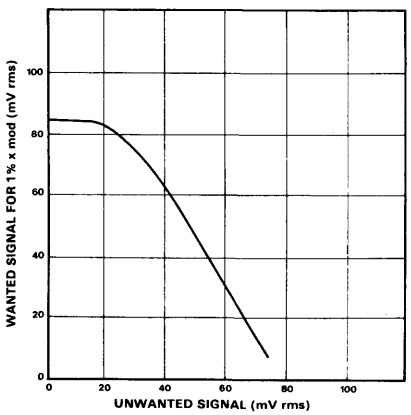


Fig. 5 Cross modulation performance (see note 1)

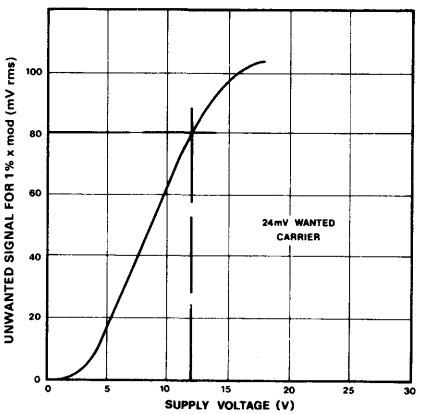


Fig. 6 Cross modulation performance V supply voltage (see note 1)

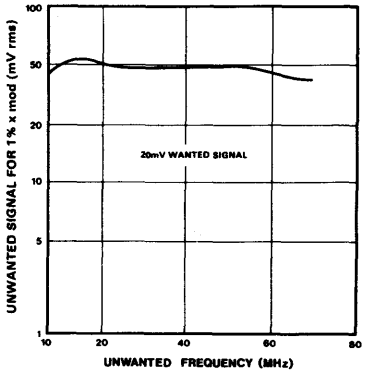


Fig. 7 Cross modulation performance V frequency of unwanted signal (see note 1)

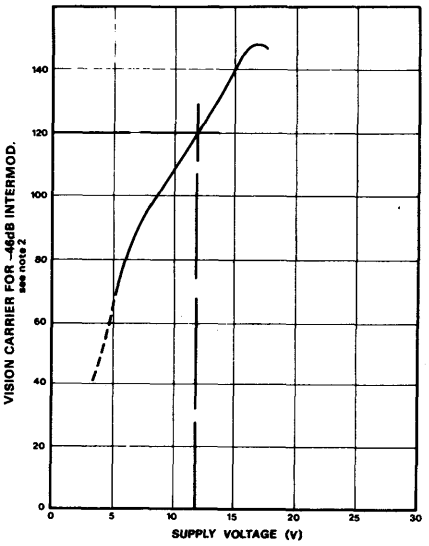


Fig. 9 Intermodulation performance v. supply voltage

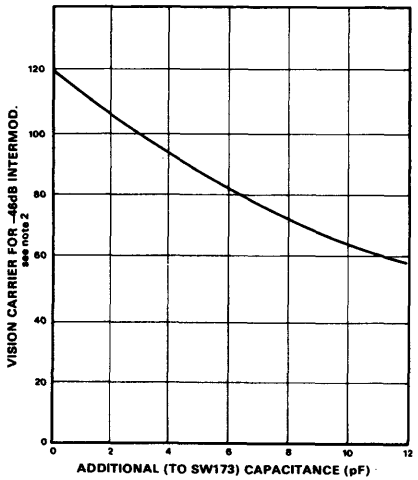


Fig. 8 Intermodulation performance v. load capacitance

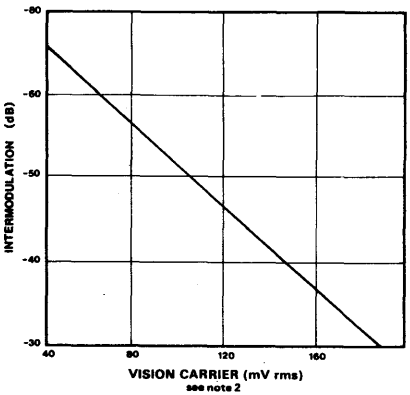


Fig. 10 Intermodulation performance (see note 2)

NOTE 1. Signal level refers to peak rms. i.e. The effective sync. tip level of a composite video signal.

NOTE 2. The test signal employed corresponds to the red bar of a transmitted colour bar and consists of the following elements related to the sync. tip level, the vision carrier at 38.9MHz–6dB, the colour carrier at 34.5MHz–18dB, and the sound carrier at 33.4MHz–7dB.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	−0.5V to +25V
Operating temperature range	−10°C to +65°C
Storage temperature range	−55°C to +125°C

PLESSEY
Semiconductors

ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have '*pre-production*' status. Details given may, therefore, change without notice although we would expect this performance data to be representative of '*full production*' status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

SL 1440

PARALLEL SOUND AND VISION IF AMPLIFIERS AND DETECTORS

This IC is designed to operate with a two output port surface acoustic wave IF filter, one output for vision and chrominance carriers with no sound carrier, and one output for the sound carrier only.

The IC amplifies and detects the sound and vision carrier in two separate channels, the detectors being of the wide band switching type, not requiring any tuning. An AGC system is applied to the vision channel, the sound channel being made to hard limit.

If there is no facility for tuner AGC, an SL1431 should be used to provide this signal, operating before the SWAF to provide superior overload performance and needing no preset adjustment.

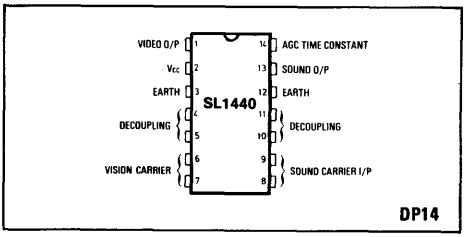


Fig. 1 Pin connections (top view)

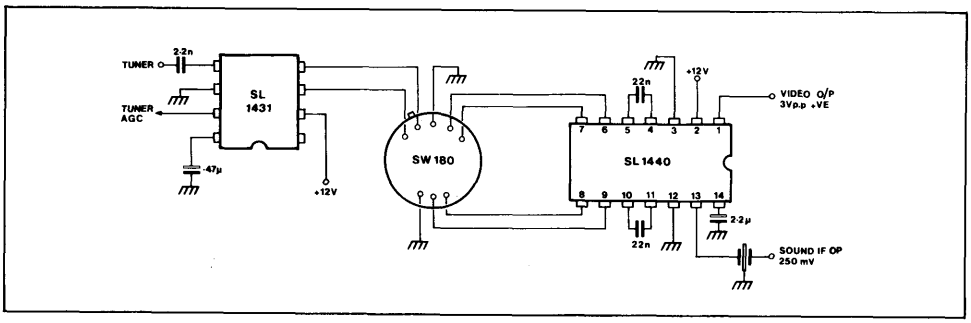


Fig. 2 Typical application SL1440

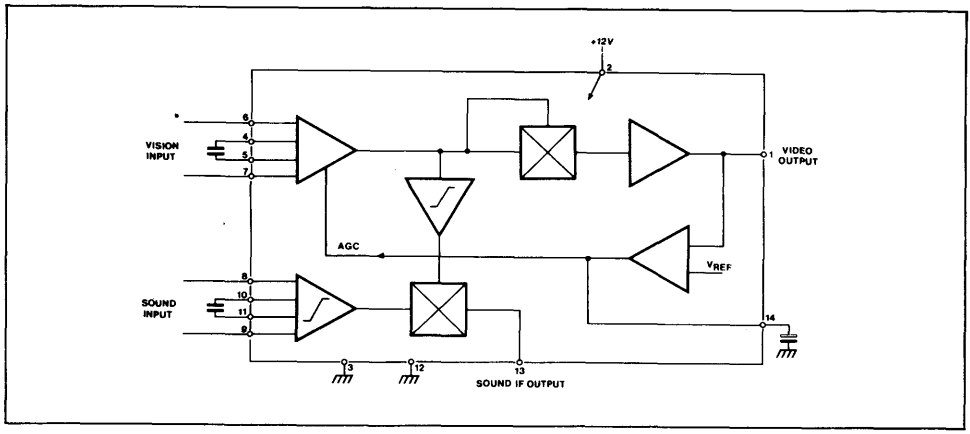


Fig. 3 IC block diagram.

PLESSEY
Semiconductors

SP4020/1

VHF/UHF 1 GHz ÷ 64

The SP4020 and SP4021 are ECL divide by 64s which will operate at frequencies in excess of 950MHz, and are intended for use as prescalers in television receiver synthesiser tuners.

The SP4020 has separate inputs for VHF and UHF and the devices have a typical power dissipation of 470mW at the nominal supply voltage of +6.8V.

FEATURES

- Dual Input Ports for VHF and UHF (SP4020)
- Self-Biasing Clock Inputs
- Variable Input Hysteresis Capability for Wide Band Operation
- TTL/MOS Compatible Band Change Input (SP4020)
- Push-Pull TTL O/P

OPERATING NOTES

Two input ports are available on the SP4020. Switching between these inputs is accomplished by operation of the band change input. A logic '1' activates the UHF input, logic '0' the VHF input. When an input is not in use the input signal must be removed to prevent cross-modulation occuring at high frequencies. Both inputs are terminated by a nominal 400 Ω and should be AC coupled to their respective signal sources. Input power to the device is terminated to ground by the two decoupling capacitors on the reference pins. Input coupling and reference decoupling capacitors should be of a type suitable for use at a frequency of 1GHz.

When the device is switched to the VHF input, an input hysteresis of 50mV is set by the internal band change circuit. This improves the low frequency sinewave operation of the device. The hysteresis level may be measured as $V_{REF1} - V_{REF2}$

If the SP4021 is required to operate with a sinewave input below 100MHz, then the required hysteresis may be applied externally as shown in Fig. 5. Large values of hysteresis should be avoided as this will degrade the input sensitivity of the device at the maximum frequency. The divide by 64 output is designed to interface with TTL which has a common V_{EE} (ground). At low frequency the output will change when one of the clock change inputs changes from a low to a high level. Self oscillation may result if the input signal falls below the minimum specified.

The devices may be operated down to very low frequencies if a square wave input with an edge speed greater than 200V/μs is used.

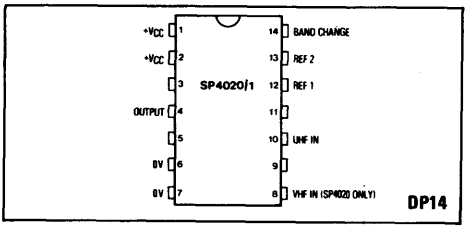
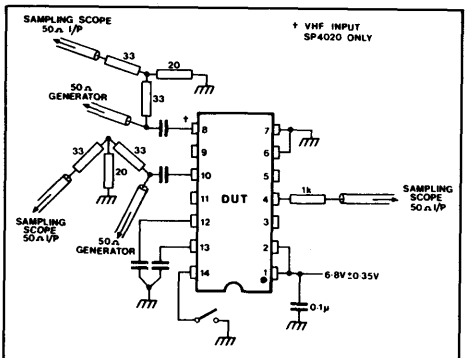
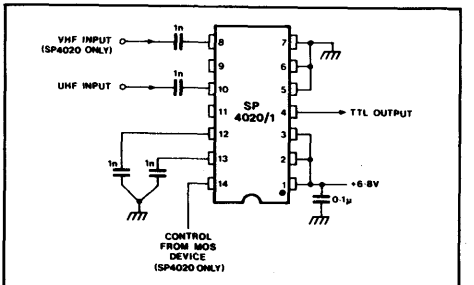


Fig. 1 Pin connections



Only one generator should be connected to either the VHF or UHF inputs. The input not in use may be left open circuit. All capacitors are 1nF unless otherwise stated.

Fig.2 AC test circuit



Connections to these pins should be made to have the minimum series inductance. Capacitors should be of a type suitable for use at 1GHz.

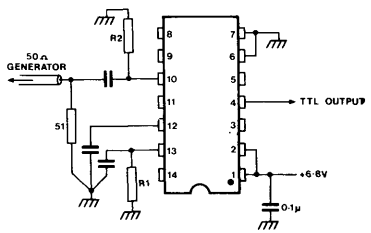
Fig.3 Application circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{EE} = oV, Vcc = +6.45V to +7.15V
Clock input voltage sinusoidal
T_A: +25°C
Pin 14 O/P

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	1,2	6.45	6.80	7.15	V	
Supply current	1,2	40	68	90	mA	Vcc = 6.8V
Output level high	4	2.5	3.5	5.0	V	−1mA
Output level low	4		0.3	0.5	V	5mA
Band change input (SP4020 only)						See Note 1
High level	14	2.5			V	For UHF input
Low level	14			0.4	V	For VHF input
Low level I/P current	14			−0.8	mA	@ 0.4V
Max. clamp current	14	−3			mA	@ −0.7V
Sensitivity						
SP4020:-						
VHF I/P 100MHz	8		100	300	mVp–p	Pin 14 to 0V
VHF I/P 300MHz			50	300	mVp–p	Pin 14 to 0V
UHF I/P 500–800MHz	10		100	300	mVp–p	
UHF I/P 950MHz			50	300	mVp–p	See Note 2
SP4021:-						
I/P 100MHz	10		120	400	mVp–p	
I/P 300–800MHz			100	300	mVp–p	
I/P 950MHz			50	300	mVp–p	See Note 2
Overload level						
SP4020:-						
VHF I/P 100–300MHz	8	0.9	2.0		Vp–p	
UHF I/P 100–950MHz	10	0.9	2.0		Vp–p	Pin 14 to 0V
SP4021:-						
I/P 100–300MHz	10	1.0	2.0		Vp–p	
I/P 500–950MHz	10	0.9	2.0		Vp–p	

Note 1 TTL type including negative input voltage clamp
Note 2 This is measured with the device in a low profile socket; soldered results show, typically, a 25% improvement.



Capacitors are 1nF unless otherwise stated. Values should be increased if operation below 10MHz is required.

For 50mV hysteresis R1 = 36kΩR2 = ∞
For 100mV hysteresis R1 = 18kΩR2 = 18kΩ

Fig. 4 Wideband operation

ABSOLUTE MAXIMUM RATINGS

Power supply voltage Vcc − V_{EE}	0V to +10V
Input voltage, clock inputs	2.5V p–p
Band change input (SP4020)	+7.2 to −0.5V or −10mA
Output current	+30mA to −30mA
Operating temperature	0°C to +65°C
Storage temperature	−55°C to +125°C

PLESSEY
Semiconductors

SP4040/1

VHF/UHF 1 GHz ÷ 256

The SP4040 and SP4041 are ECL divide by 256 which will operate at frequencies in excess of 950MHz, and are intended for use as prescalers in television receiver synthesiser tuners.

The SP4040 has separate inputs for VHF and UHF and the devices have a typical power dissipation of 500mW at the nominal supply voltage of +6.8V.

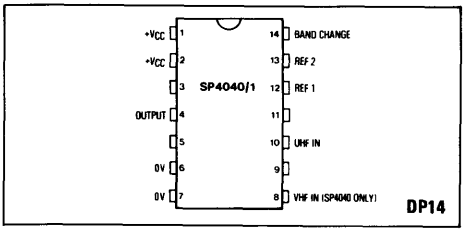


Fig. 1 Pin connections

FEATURES

- Dual Input Ports for VHF and UHF (SP4040)
- Self-Biasing Clock Inputs
- Variable Input Hysteresis Capability for Wide Band Operation
- TTL/MOS Compatible Band Change Input (SP4040)
- Push-Pull TTL O/P

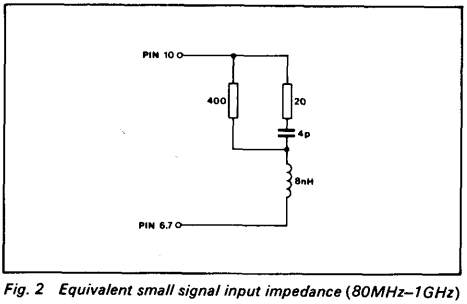


Fig. 2 Equivalent small signal input impedance (80MHz–1GHz)

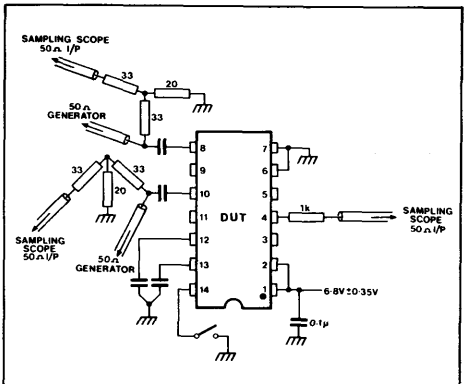
OPERATING NOTES

Two input ports are available on the SP4040. Switching between these inputs is accomplished by operation of the band change input. A logic '1' activates the UHF input, logic '0' the VHF input. When an input is not in use the input signal must be removed to prevent cross-modulation occuring at high frequencies. Both inputs are terminated by a nominal 400 Ω and should be AC coupled to their respective signal sources. Input power to the device is terminated to ground by the two decoupling capacitors on the reference pins. Input coupling and reference decoupling capacitors should be of a type suitable for use at a frequency of 1GHz.

When the device is switched to the VHF input, an input hysteresis of 50mV is set by the internal band change circuit. This improves the low frequency sinewave operation of the device. The hysteresis level may be measured as $V_{REF\,1} - V_{REF\,2}$

If the SP4041 is required to operate with a sinewave input below 100MHz, then the required hysteresis may be applied externally as shown in Fig. 5. Large values of hysteresis should be avoided as this will degrade the input sensitivity of the device at the maximum frequency. The divide output is designed to interface with TTL which has a common V_{EE} (ground). At low frequency the output will change when one of the clock change inputs changes from a low to a high level. Self oscillation may result if the input signal falls below the minimum specified.

The devices may be operated down to very low frequencies if a square wave input with an edge speed greater than 200V/μs is used.



Only one generator should be connected to either the VHF or UHF inputs. The input not in use may be left open circuit. All capacitors are 1nF unless otherwise stated.

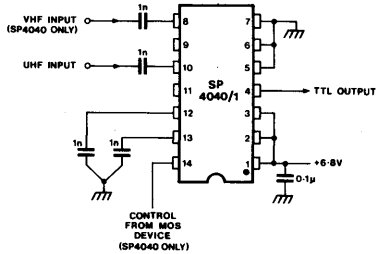
Fig. 3 AC test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{EE} = oV, Vcc = +6.45V to +7.15V
Clock input voltage sinusoidal
T_A: +25°C
Pin 14 O/P

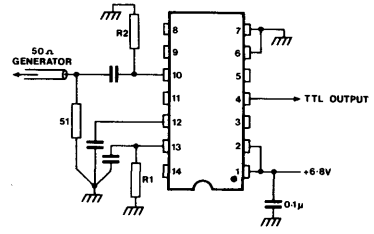
Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	1,2	6.45	6.80	7.15	V	
Supply current	1,2		65	90	mA	V_{CC} = 6.8V
Output level:						
High	4	2.4	3.5	5.0	V	2mA
Low	4		0.3	0.4	V	5mA
Band change input						
High level	14	2.5			V	For UHF input } SP4040 only
Low level	14			0.4	V	For VHF input } SP4040 only
Low level I/P current	14			–0.8	mA	@ 0.4V } SP4040 only
Max. clamp current	14	–3			mA	@ –0.7V } SP4040 only
Sensitivity						
SP4040:-						
VHF I/P 100MHz	8		40	100	mV	Pin 14 to 0V
300MHz			35	100	mV	Pin 14 to 0V
UHF I/P 500–800MHz	10		35	100	mV	
950MHz	10		90	155	mV	Note 1
SP4041:-						
100MHz	10		140	200	mV	
200MHz	10		100	140	mV	
300MHz	10		50	125	mV	
400-700MHz	10		35	100	mV	
800MHz	10		70	140	mV	
950MHz	10		140	250	mV	Note 1
Overload level						
SP4040:-						
VHF I/P 100–300MHz	8	350	700		mV	
UHF I/P 500–600MHz	10	350	700		mV	Pin 14 to 0V
SP1041:-						
100MHz	10	425	700		mV	
300MHz	10	350	700		mV	
500–600MHz	10	350	700		mV	
950MHz	10	425	880		mV	

Note 1. This is measured with the device in a low profile socket; soldered in results show typically a 25% improvement.



Connections to these pins should be made to have the minimum series inductance. Capacitors should be of a type suitable for use at 1GHz.

Fig. 4 Application circuit



Capacitors are 1nF unless otherwise stated. Values should be increased if operation below 10MHz is required.

For 50mV hysteresis R1 = 36kΩR2 = ∞
For 100mV hysteresis R1 = 18kΩR2 = 18kΩ

Fig. 5 Wideband operation

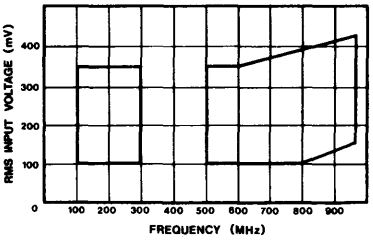


Fig. 6 SP4040 typical sensitivity with limits of operation when used in application circuit (Fig. 4)

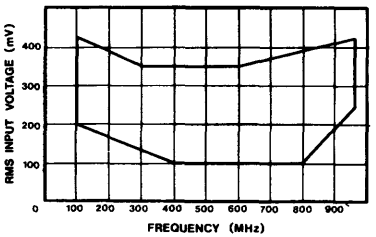


Fig. 7 SP4041 Typical sensitivity with limits of operation when used in application circuit (Fig. 4) with pin 14 open circuit.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	0V to +10V
Input voltage, clock inputs	880mV
Band change input	+7.2V
(SP4040)	−10mA
Output current	+30mA to −30mA
Operating temperature	0°C to +65°C
Storage temperature	−55°C to +125°C

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SP4531

1 GHz ÷ 64

The SP4531 is one of the new range of Plessey Consumer high speed dividers which offer improved input sensitivity and input impedance characteristics.

The device is intended for use in television frequency synthesis systems. It has a division ratio of 64 with dual ECL outputs and incorporates an on-chip preamplifier with a differential input. The input pins may be used as UHF and VHF inputs, with only a slight loss of sensitivity, if suitable drive circuitry is employed.

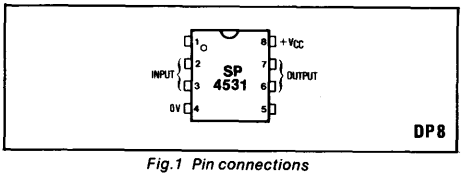

Fig.1 Pin connections

FEATURES

- On-chip wideband amplifier
- High input sensitivity
- High input impedance
- Low output radiation
- Complementary ECL output

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7V
Input voltage	2.5V p-p
Ambient operating temperature	-10°C to +65°C
Storage temperature	-55°C to +125°C

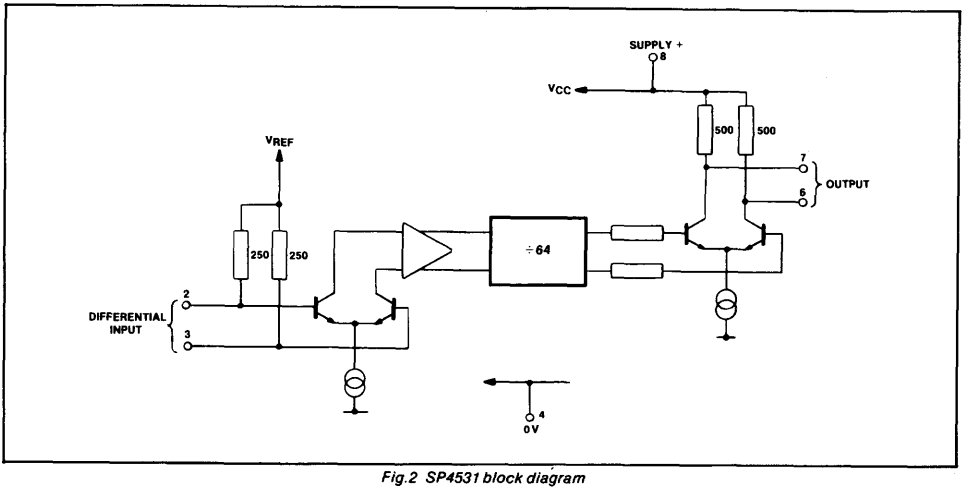

Fig.2 SP4531 block diagram

ELECTRICAL CHARACTERISTICS (see Fig.3)

Test Conditions (unless otherwise stated):
$T_{amb} = +25°C$, $V_{CC} = +5V$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range	8	4.5	5	5.5	V	
Supply current	8		60	80	mA	
Input voltage, V_{IN}, 80MHz	2	17.5		200	mVrms	Sine wave into 50Ω
300MHz	2	17.5		200	mVrms	
500MHz	2	17.5		200	mVrms	
700MHz	2	17.5		200	mVrms	
1GHz	2	17.5		200	mVrms	
Output voltage	6	0.8			Vp-p	No load
	7	0.8			Vp-p	
Output imbalance	6, 7			0.1	V	
Output impedance	6		500		Ω	
	7		500		Ω	

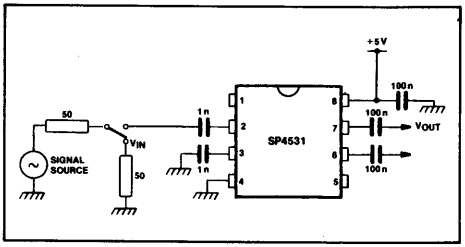

Fig.3 Test configuration

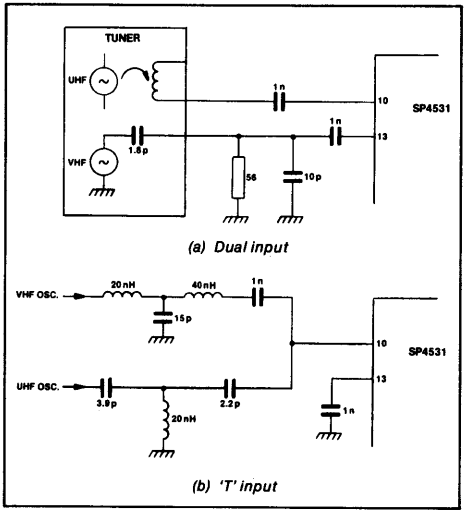

Fig.4 Combined input operation

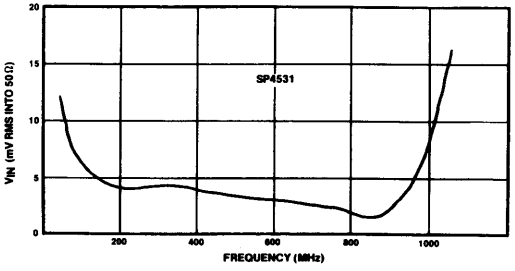

Fig.5 Typical input sensitivity

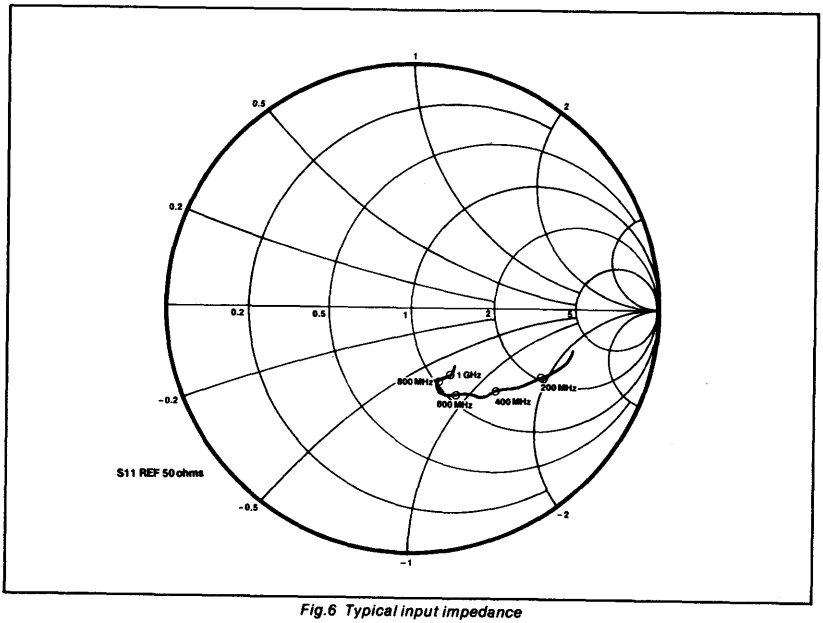

Fig.6 Typical input impedance

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SP4541

1 GHz ÷ 256

The SP4541 is one of the new range of Plessey Consumer high speed dividers which offer improved input sensitivity and input impedance characteristics.

The device is intended for use in television frequency synthesis systems. It has a division ratio of 256 with a single TTL output and incorporates an on-chip preamplifier with a differential input. The input pins may be used as UHF and VHF, with only a slight loss of sensitivity, if suitable drive circuitry is employed.

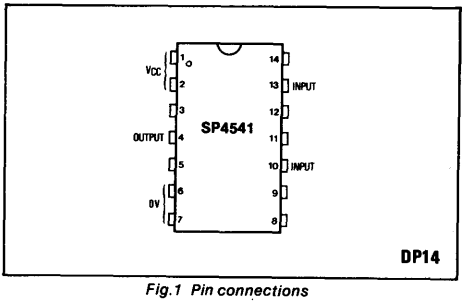

Fig.1 Pin connections

FEATURES

- On-chip wideband amplifier
- High input sensitivity
- High input impedance
- Low output radiation
- TTL output

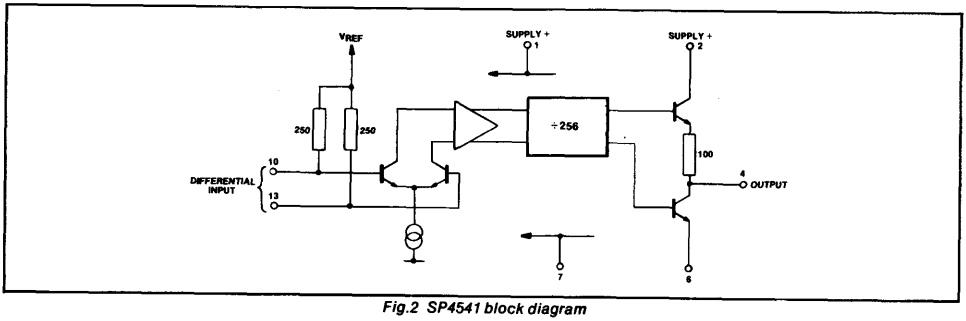

Fig.2 SP4541 block diagram

ELECTRICAL CHARACTERISTICS (see Fig.3)

Test Conditions (unless otherwise stated):
$T_{amb} = +25°C$, $V_{CC} = +5V$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range	1, 2	4.5	5	5.5	V	
Supply current	1, 2		70	90	mA	
Input voltage, V_{IN}, 80MHz	10	17.5		200	mVrms	Sine wave into 50Ω
300MHz	10	17.5		200	mVrms	
500MHz	10	17.5		200	mVrms	
700MHz	10	17.5		200	mVrms	
1000MHz	10	17.5		200	mVrms	
Output voltage High		3.3			V	Sourcing 0.2mA
Low				0.4	V	Sinking 2mA

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7V
Input voltage	2.5V p-p
Ambient operating temperature	-10°C to +65°C
Storage temperature	-55°C to +125°C

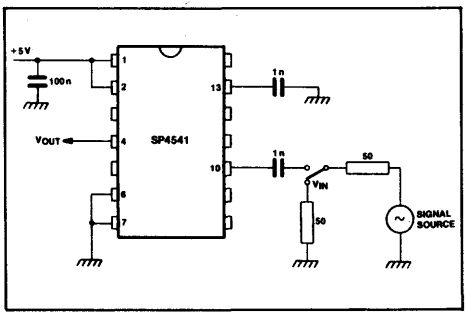

Fig.3 Test configuration

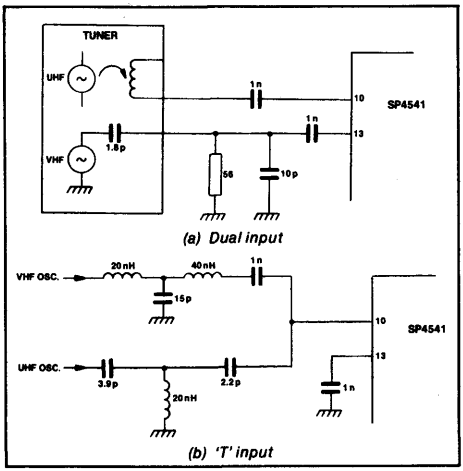

Fig.4 Combined input operation

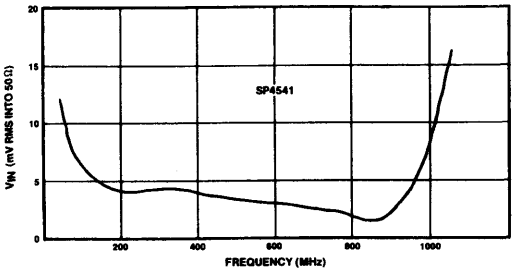

Fig.5 Typical input sensitivity

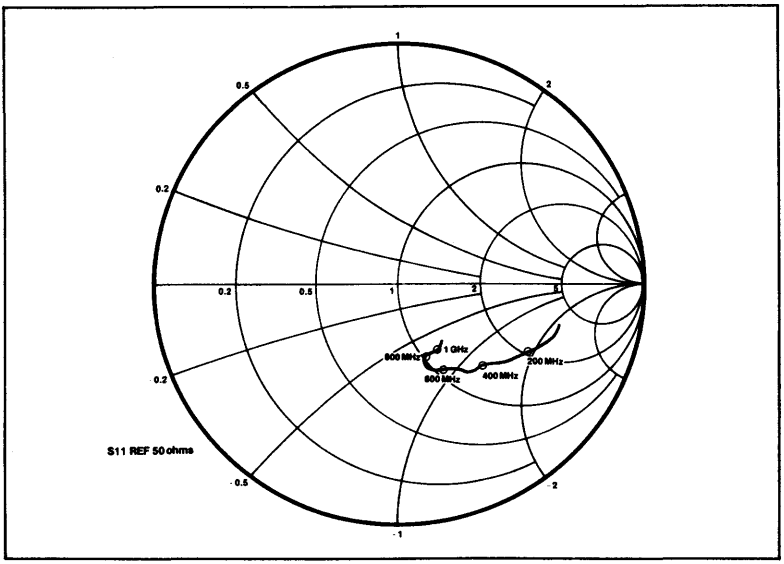

Fig.6 Typical input impedance

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SP4545

COMBINED VHF ÷ 64, UHF ÷ 256

The SP4545 is one of the new range of Plessey Consumer high speed dividers which offer improved input sensitivity and input impedance characteristics.

The device is intended for use in television frequency synthesis systems. It has a division ratio of 64 for VHF input and 256 for UHF input, the VHF input incorporates an on-chip preamplifier with a differential input. The VHF input is selected when the band select is low and when it is high the UHF input is selected.

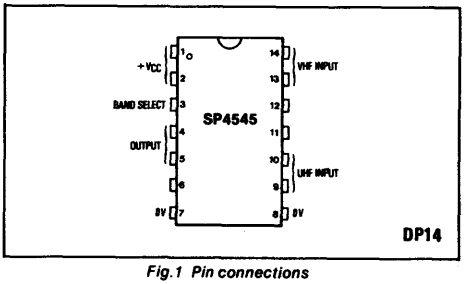

Fig.1 Pin connections

FEATURES

- On-chip wideband amplifier
- High input sensitivity
- High input impedance
- Low output radiation
- Complementary ECL output
- Separate VHF and UHF inputs
- ÷64 for VHF
- ÷256 for UHF
- On-chip input selection

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7V
Input voltage	2.5V p-p
Ambient operating temperature	-10°C to 65°C
Storage temperature	-55°C to 125°C

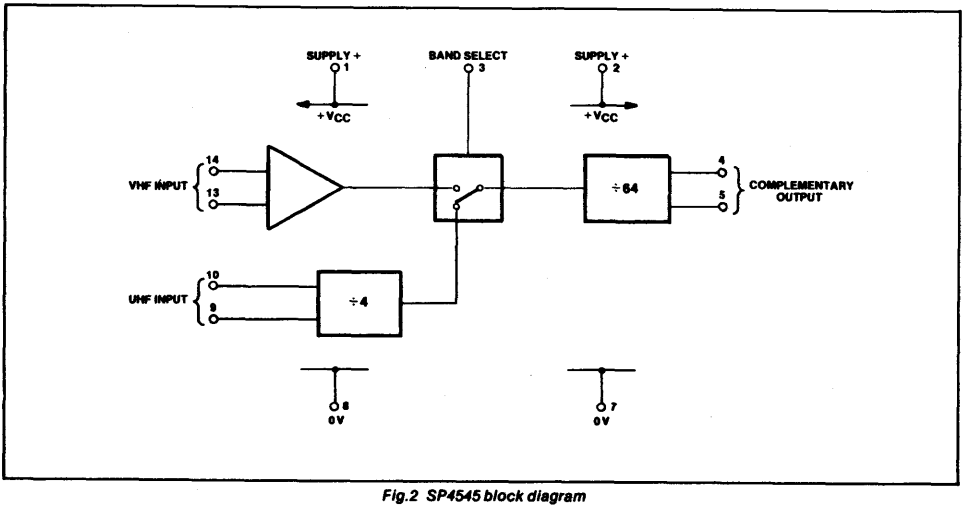

Fig.2 SP4545 block diagram

ELECTRICAL CHARACTERISTICS (see Fig.3)

Test Conditions (unless otherwise stated):
$T_{amb} = +25°C$, $V_{CC} = +5V$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range	1, 2	4.5	5	5.5	V	
Supply current	1, 2		60	90	mA	
Input voltage, V_{IN}, 80MHz	13	17.5		200	mVrms	Pin 3 low (÷64)
(rms sine wave 300MHz	13	17.5		200	mVrms	
into 50Ω) 240MHz	10	50		200	mVrms	Pin 3 high (÷256)
600MHz	10	40		200	mVrms	
1000MHz	10	40		200	mVrms	
Output voltage	4	0.8			Vp-p	No load
	5	0.8			Vp-p	
Output imbalance	4, 5			0.1	Vp-p	
Output impedance			200		Ω	
			200		Ω	
Band select input voltage high	3	2		20.5	V	UHF
low	3			0.8	V	VHF
current high	3			500	μA	Sinking
low	3			100	μA	Sourcing

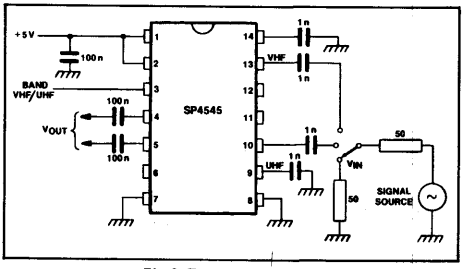

Fig.3 Test configuration

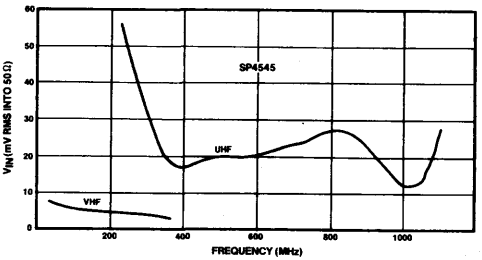

Fig.4 Typical input sensitivity

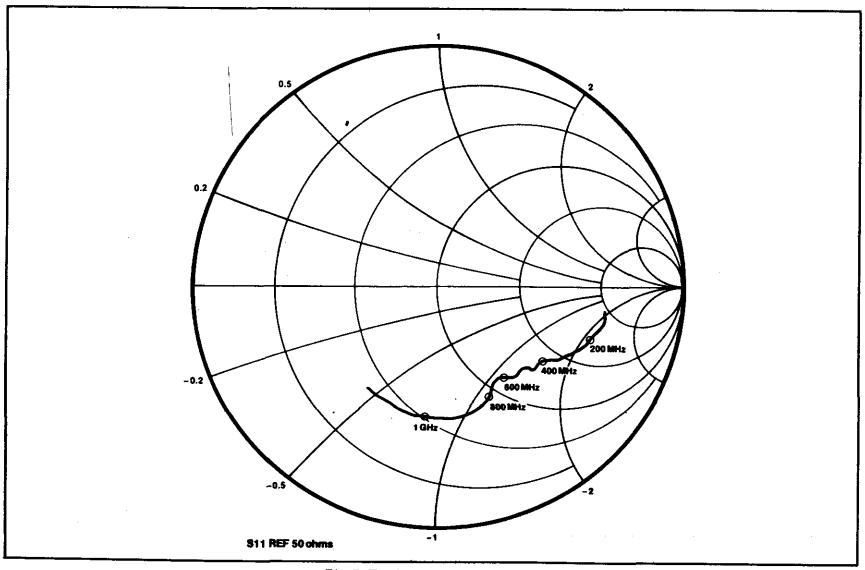

Fig.5 Typical input impedance

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SP4550/1

1 GHz ÷ 256

The SP4550/1 are part of the new range of Plessey Consumer high speed dividers which offer improved input sensitivity and higher input impedance.

The devices are intended for use in television frequency synthesis systems. They have a division ratio of 256 with a single, (SP4550) or complementary, (SP4551) ECL output and incorporate an on-chip preamplifier with a differential input. The input pins may be used as UHF and VHF inputs, with only a slight loss of sensitivity, if suitable drive circuitry is employed.

FEATURES

- On-chip wideband amplifier
- High input sensitivity
- High input impedance
- Low output radiation
- Single (SP4550) or complementary (SP4551) ECL output

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7V
Input voltage	2.5V p-p
Ambient operating temperature	-10°C to +65°C
Storage temperature	-55°C to +125°C

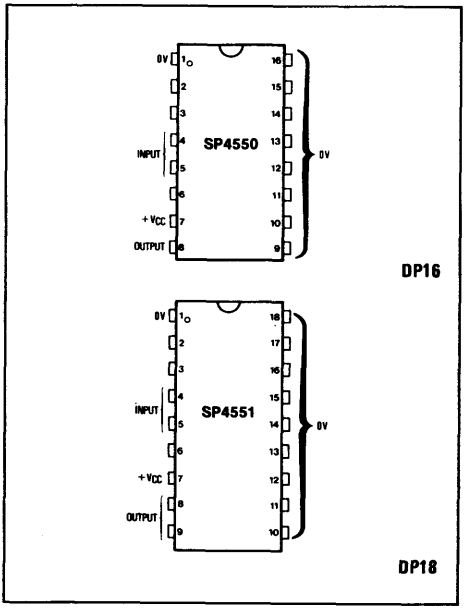

Fig.1 Pin connections

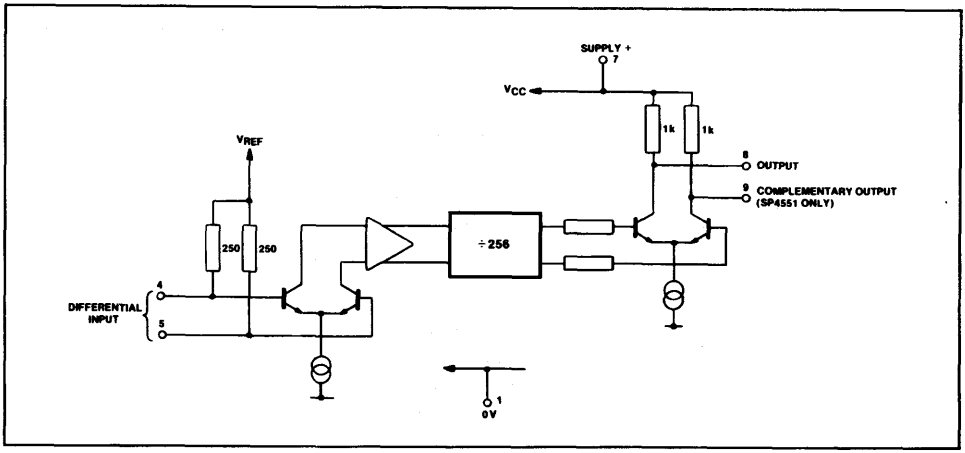

Fig.2 SP4550/1 block diagram

ELECTRICAL CHARACTERISTICS (see Fig.3)

Test Conditions (unless otherwise stated):
$T_{amb} = +25°C$, $V_{CC} = +5V$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range	7	4.5	5	5.5	V	
Supply current	7		60	90	mA	
Input voltage, V_{IN}, 80MHz	4, 5	17.5		200	mVrms	Sine wave into 50Ω
300MHz		17.5		200	mVrms	
500MHz		17.5		200	mVrms	
700MHz		17.5		200	mVrms	
1000MHz		17.5		200	mVrms	
Output voltage	8	0.8			Vp-p	No load
	9	0.8			Vp-p	SP4551 only
Output imbalance	8, 9			0.1	V	SP4551 only
Output impedance	8		1		kΩ	
	9		1		kΩ	SP4551 only

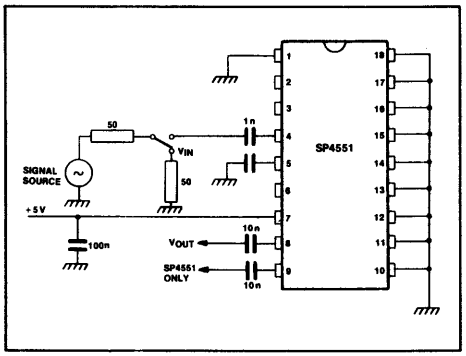

Fig.3 Test configuration

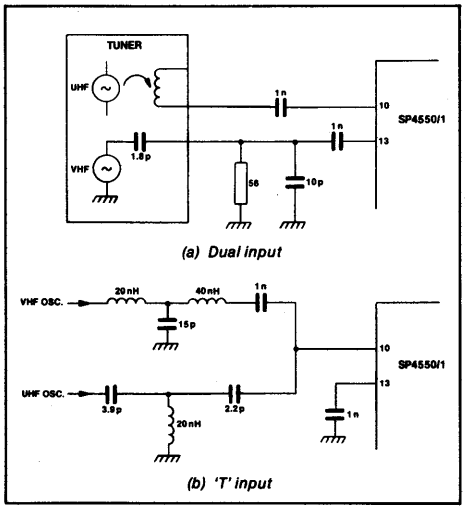

Fig.4 Combined input operation

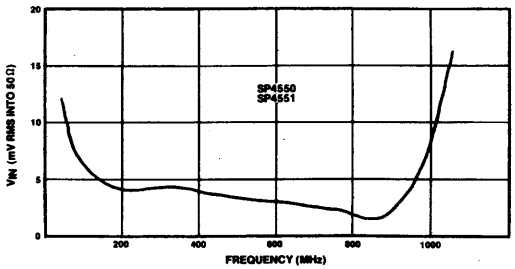

Fig.5 Typical input sensitivity

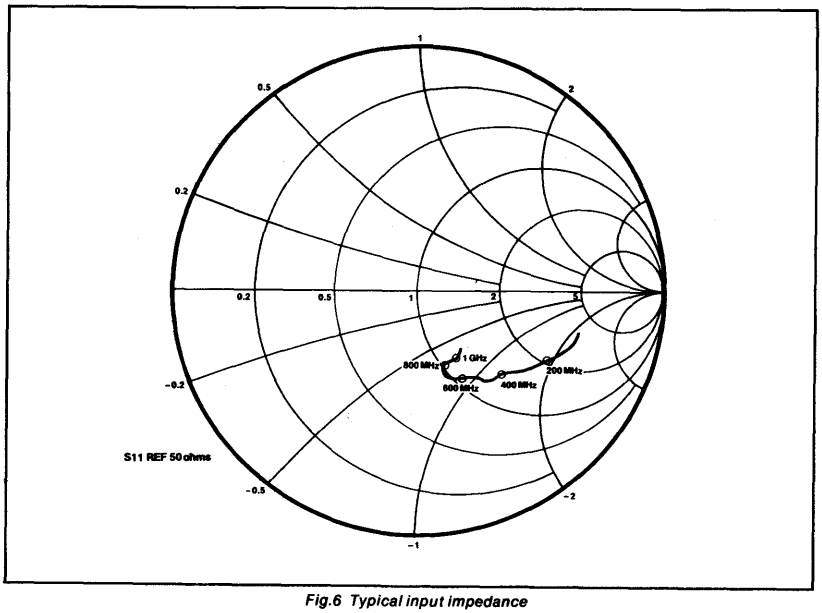

Fig.6 Typical input impedance

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SW153 SW172 SW173 SW174 SW203 SW250 SW260 SW453

SURFACE ACOUSTIC WAVE COLOUR TV IF FILTERS

This comprehensive range of TV IF filters utilises Plessey Surface Acoustic Wave technology and is suitable for use in colour or monochrome television receivers world wide. The frequency pass-band and phase response of each of these highly stable devices are tailored to the relative transmission standard. The devices require no adjustment and are packaged in a totally hermetic Metal/Glass T08 package.

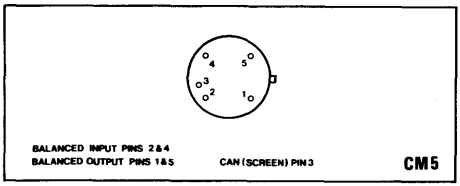


Fig. 1 Pin connections (viewed from beneath)

FEATURES

- No Adjustment Necessary
- Low Cost
- Compact Dimensions
- High Stability
- High Reliability
- Comprehensive Range of Standards Available

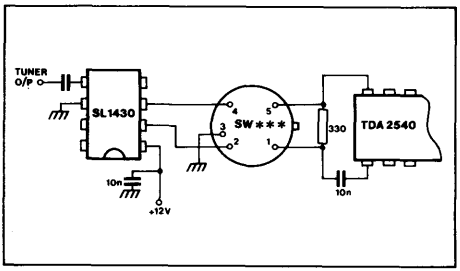


Fig. 2 Typical application

APPLICATION NOTES

The input drive and output load circuitry should provide a low impedance across at least one device port to minimise spurious signals due to secondary device characteristics. Fig. 2 shows a typical application, the SL1430 providing a very low drive impedance. The 330 Ω load resistor is included to ensure stability of the TDA2540 and may be omitted in some designs that do not use this device.

Care must be taken with the printed circuit board layout, and the use of balanced input and output is advised to ensure low levels of direct breakthrough. The device must also be mounted with minimum lead length. Application introduced direct breakthrough will exhibit itself as a deterioration in amplitude and group delay ripple, and a screen image approximately 1.5μs before the main response.

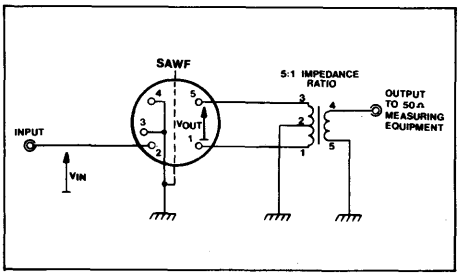


Fig. 3 Test circuit

TEST CIRCUIT

The recommended test circuit is shown in Fig.3. When used in a 50Ω system, with the input unterminated, the extra loss introduced by the test circuit is 2.5dB.

An earthed metal screen of at least 2 x 3cm should be incorporated between the leads as shown. A suitable transformer is available from MINI-CIRCUITS, New York, U.S.A., type number T5-1T.

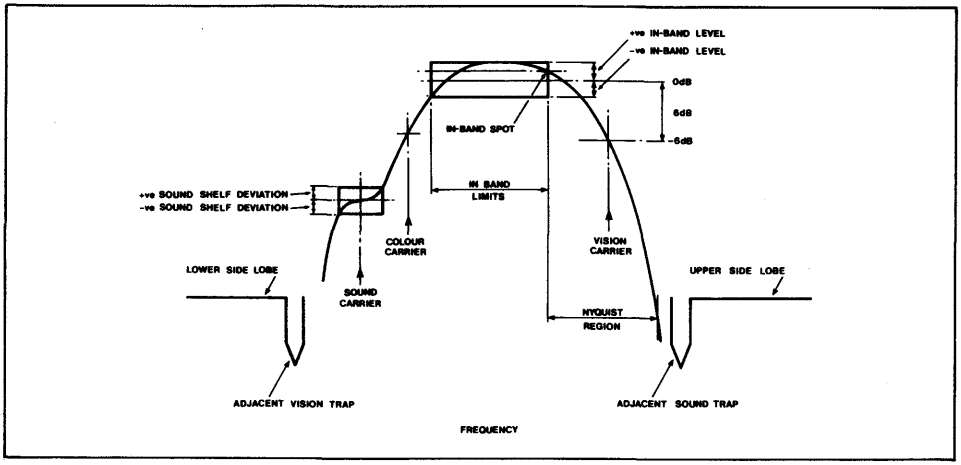


Fig. 4 Amplitude characteristics

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated) :-

Ambient temperature	+35°C
Input drive impedance	50 Ω
Load impedance	250 Ω balanced

The amplitude level at the vision carrier frequency is taken to be −6dB and is then used as a reference for all other relevant measurements (see Fig. 4).
The insertion loss is defined as the voltage ratio $2V_{IN}/V_{OUT}$ in the test circuit (Fig.3) at the vision carrier frequency and is expressed in dB. This relates to the 0dB level shown in Fig.4.

The amplitude characteristics given in the Electrical Characteristic tables are defined in Fig. 4. The response in the Nyquist region is guaranteed by the measurement of the 2T sin² pulse and bar K rating after synchronous demodulation.

In-band amplitude ripple is defined as the worst deviation from the mean over any 500kHz bandwidth between the two defined in-band frequency limits.

The measurement of spurious outputs includes those due to internal reflections and direct breakthrough, a 2T Sin² pulse being used and measurements being made between 2 and 1μs before, and 1 and 4μs after, the centre of the main response.

SW153

The SW153 is a TV IF filter for the United Kingdom PAL standard, system I, with a vision carrier frequency of 39.5MHz.

Characteristic	Frequency MHz	Value Min.	Value Typ.	Value Max.	Units	Conditions
Vision carrier	39.5		Ref. level	−6	dB	
Colour carrier	35.1	−6	−3	0	dB	
Sound carrier	33.5	−25	−22	−19	dB	
Sound shelf deviation	33.2–33.8		±1	±3	dB	
In-band level	36–38	−2	0	2	dB	
In band spot	38	−1.5	0	1.5	dB	
In-band ripple	36–38		0.5	1	dB	Peak
Adjacent vision trap	31.5	−45	−55		dB	
Adjacent sound trap	41.5	−40	−50		dB	
Lower side lobe	26.5–31.5	−40	−50		dB	
Upper side lobe	41.5–46.5	−36	−42		dB	
	46.5–100		−30		dB	
Insertion loss		18	21	24	dB	
2T sin² pulse and bar K rating	39.5		1.5	2	%	
Group delay deviation	34.5–40.5		10	40	ns	
Spurious outputs	39.5		−48	−42	dB	
Temperature coefficient of frequency			−72		ppm/°C	
Small signal impedances						
Input pins 2 & 4			1.6k Ω// 8pF			
Output pins 1 & 5			1.8k Ω// 10pF			

SW172

The SW172 is a TV IF filter for the European PAL standard systems B & G with a vision carrier frequency of 38.9MHz.

Characteristic	Frequency (MHz)	Value			Units	Conditions
		Min.	Typ.	Max.		
Vision Carrier	38.9		Ref. level -6		dB	
Colour Carrier	34.5	-5	-3	-1	dB	
Sound Carrier	33.4		-27	-24	dB	
Sound Shelf	33.1 to 33.5		-28	-20	dB	
In-band level	35.5 to 37.4	-1.5	0	1.5	dB	
In-band ripple	35.5 to 37.4		0.5	1	dB	Peak
Adjacent vision trap						
UHF	30.9	-42	-48		dB	
VHF	31.8 to 32	-46	-50		dB	
Adjacent sound trap						
VHF	40.3 to 40.5	-42	-46		dB	
UHF	41.4	-40	-44		dB	
Lower side lobe	27.5 to 31.9	-40	-44		dB	
Upper side lobe	40.4 to 45	-38	-42		dB	
	45 to 100		-30		dB	
Insertion loss		18	20	23	dB~	
2Tsin² pulse and bar K rating	38.9		2	3	%	
Group delay deviation	34.1		80		ns	Reference 0 @ 38.9MHz
	34.5	40	60	80	ns	Reference 0 @ 38.9MHz
	34.15		0		ns	Reference 0 @ 38.9MHz
	36.9		-90		ns	Reference 0 @ 38.9MHz
	37.9		-55		ns	Reference 0 @ 38.9MHz
	39.9		-20		ns	Reference 0 @ 38.9MHz
Spurious outputs	38.9		-48	-42	dB	
Temperature Coefficient of frequency			-90		ppm/°C	
Small signal impedances						
Input pins 2 & 4			1.6kΩ// 10pf			
Output pins 1 & 5			1kΩ// 12pf			

SW173

The SW173 is a TV IF filter for the European PAL standard, systems B and G, with a vision frequency of 38.9MHz

Characteristic	Frequency MHz	Value			Units	Conditions
		Min.	Typ.	Max.		
Vision carrier	38.9		Ref. level –6		dB	
Colour carrier	34.5	–5	–3	–1	dB	
Sound carrier	33.4	–23	–20	–17	dB	
Sound shelf deviation	33.1–33.5		±2	±4	dB	
In-band level	35.5–37.4	–2	0	2	dB	
In-band spot	37.4	-1.5	0	1.5	dB	
In-band ripple	35.5–37.4		0.75	1.5	dB	Peak
Adjacent vision trap						
UHF	30.9	–40	–43		dB	
VHF	31.9	–42	–46		dB	
Adjacent sound trap						
VHF	40.4	–42	–46		dB	
UHF	41.4	–40	–43		dB	
Lower side lobe	27.5–31.9	–37	–42		dB	
Upper side lobe	40.4–45	–37	–42		dB	
	45–100		–30		dB	
Insertion loss		18	20	23	dB	
2T sin² pulse and bar K rating	38.9		2	3	%	

SW173 (Continued)

Characteristic	Frequency MHz	Value Min.	Value Typ.	Value Max.	Units	Conditions
Group delay deviation	34.1		400		ns	Reference 0 @ 38.9MHz
	34.5		170		ns	Reference 0 @ 38.9MHz
	35.15		0		ns	Reference 0 @ 38.9MHz
	36.9		−90		ns	Reference 0 @ 38.9MHz
	37.9		−53		ns	Reference 0 @ 38.9MHz
	39.9		−53		ns	Reference 0 @ 38.9MHz
Spurious outputs	38.9		−48	−42	dB	
Temperature coefficient of frequency			−72		ppm/°C	
Small signal impedances						
Input pins 2 & 4			1.6kΩ// 8pF			
Output pins 1 & 5			1.8kΩ// 10pF			

SW174 ADVANCE INFORMATION *

The SW174 is a TV IF filter for the European PAL standard systems B & G with a vision carrier frequency of 38.9MHz

Characteristic	Frequency MHz	Value Min.	Value Typ.	Value Max.	Units	Conditions
Vision Carrier	38.9		Ref. level −6		dB	
Colour Carrier	34.5	−4	−2	0	dB	
Sound Carrier	33.4	−23	−20	−17	dB	
Sound Shelf deviation	32.8 to 33.5		+2/−4	+4/−6	dB	
In-band level	35.5 to 37.4	−1.5	0	1.5	dB	
In-band ripple	35.5 to 37.4		0.5	1	dB	Peak
Adjacent vision trap						
UHF	30.9	−42	−48		dB	
VHF	31.8 to 32	−46	−50		dB	
Adjacent sound trap						
VHF	40.1 to 40.3	−40	−46		dB	
	40.3 to 40.5	−46	−50		dB	
UHF	41.4	−40	−44		dB	
Lower side lobe	27.5 to 31.9	−40	−46		dB	
Upper side lobe	40.4 to 45	−38	−42		dB	
	45 to 100		−30		dB	
Insertion loss		18	20	23	dB	
2Tsin² pulse and bar K rating	38.9		2	3	%	
Group delay deviation	34.1		80		ns	Reference 0 @ 38.9MHz
	34.5	40	60	80	ns	Reference 0 @ 38.9MHz
	35.15		0		ns	Reference 0 @ 38.9MHz
	36.9		−90		ns	Reference 0 @ 38.9MHz
	37.9		−55		ns	Reference 0 @ 38.9MHz
	39.9		−20		ns	Reference 0 @ 38.9MHz
Spurious outputs	38.9		−48	−42	dB	
Temperature Coefficient of frequency			−90		ppm/°C	
Small signal impedances						
Input pins 2 & 4			1.6kΩ// 10pf			
Output pins 1 & 5			1kΩ// 12pf			

* Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

SW203

The SW203 is a TV IF filter for the North American NTSC standard systems M & N with a vision carrier frequency of 45.75 MHz.

Characteristic	Frequency MHz	Value Min.	Value Typ.	Value Max.	Units	Conditions
Vision Carrier	45.75		Ref. level -6		dB	
Colour Carrier	42.17	-6	-3	0	dB	
Sound Carrier	41.25	-23	-19	-15	dB	
In-band level	43 to 44.25	-2	0	2	dB	
In-band ripple	43 to 44.25		0.5	1.5	dB	Peak
Adjacent vision trap	39.75	-40	-50		dB	
Adjacent sound trap	47.5	-38	-46		dB	
Lower side lobe	35 to 39.75	-35	-40		dB	
Upper side lobe	47.5 to 52.5	-35	-40		dB	
	52.5 to 125		-30		dB	
Insertion loss		12	15	20	dB	
2Tsin² pulse and bar K rating	45.75		2	3	%	
Group delay deviation	43 to 44.25		20		ns	
Spurious outputs			-46	-40	dB	
Temperature Coefficient of frequency			-72		ppm/°C	
Small signal impedances						
Input pins 2 & 4			1kΩ// 13pf			
Output pins 1 & 5			1.5kΩ// 11pf			

SW250 ADVANCE INFORMATION

The SW250 is a TV IF filter for the French SECAM standard systems L & L' with a vision carrier frequency of 32.7 MHz.

Characteristic	Frequency MHz	Value Min.	Value Typ.	Value Max.	Units	Conditions
Vision Carrier	32.7		Ref. level -6		dB	
Colour Carrier	37	-2	-0.5	1	dB	
	38	-3	-6	-9	dB	
In-band level	34.5 to 36	-2	0	2	dB	
In-band ripple	34.5 to 36		1	1.5	dB	Peak
Adjacent vision trap	40.7	-38	-43		dB	
Adjacent sound trap	31.2	-46	-50		dB	
Own Sound UHF	39.2	-43	-46		dB	
VHF	43.85	-43	-46		dB	
Lower side lobe	26 to 31.2	-38	-42		dB	
Upper side lobe	39.2 to 45	-38	-42		dB	
	45 to 90		-30		dB	
Insertion loss		19	22	25	dB	
2Tsin² pulse and bar K rating			2	3	%	
Group delay deviation	34.5 to 36		15	50	ns	
Spurious outputs	32.7		-48	-42	dB	
Temperature Coefficient of frequency			-90		ppm/°C	
Small signal impedances						
Input pins 2 & 4			1.6kΩ// 10pf			
Output pins 1 & 5			1.2kΩ// 11pf			

SW260 ADVANCE INFORMATION

The SW260 is a TV IF filter for the Eastern European SECAM standard system D and compatible with systems B and G with a vision carrier frequency of 38MHz.

Characteristic	Frequency MHz	Value Min.	Value Typ.	Value Max.	Units	Conditions
Vision Carrier	38		Ref. level -6		dB	
Colour Carrier	33.1	-6	-3	0	dB	
	33.7	-4	-2	0	dB	
Sound Carrier	31.5	-24	-21	-18	dB	
Sound Shelf	31.3 to 32.5	-27		-15	dB	
In-band level	34.5 to 36.5	-2	0	+2	dB	
In-band ripple	34.5 to 36.5		1	2	dB	Peak
Adjacent vision trap	30	-43	-50		dB	
Adjacent sound trap	39.5	-40	-46		dB	
Lower side lobe	25.5 to 30	-37	-42		dB	
Upper side lobe	39.5 to 44.5	-37	-42		dB	
	44.5 to 100		-30		dB	
Insertion loss		18	20	24	dB	
2Tsin² pulse and bar K rating	38		2	3	%	
Group delay deviation	32.5 to 39		15	50	ns	
Spurious outputs	38		-46	-40	dB	
Temperature Coefficient of frequency			-72		ppm/°C	
Small signal impedances						
Input pins 2 & 4			1.6kΩ// 8pf			
Output pins 1 & 5			1.8kΩ// 10pf			

SW453 ADVANCE INFORMATION

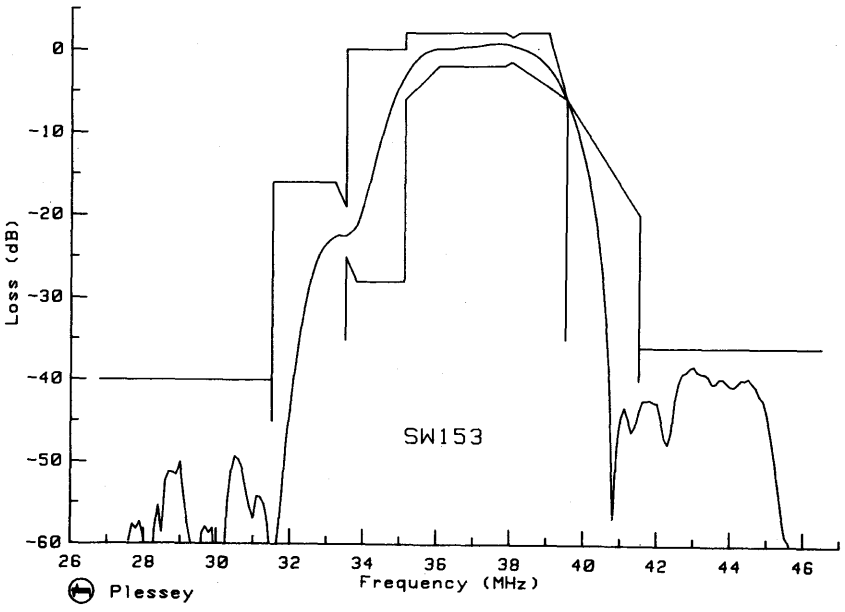
The SW453 is a TV IF filter for the South African PAL standard, system I, with a vision carrier frequency of 38.9MHz.

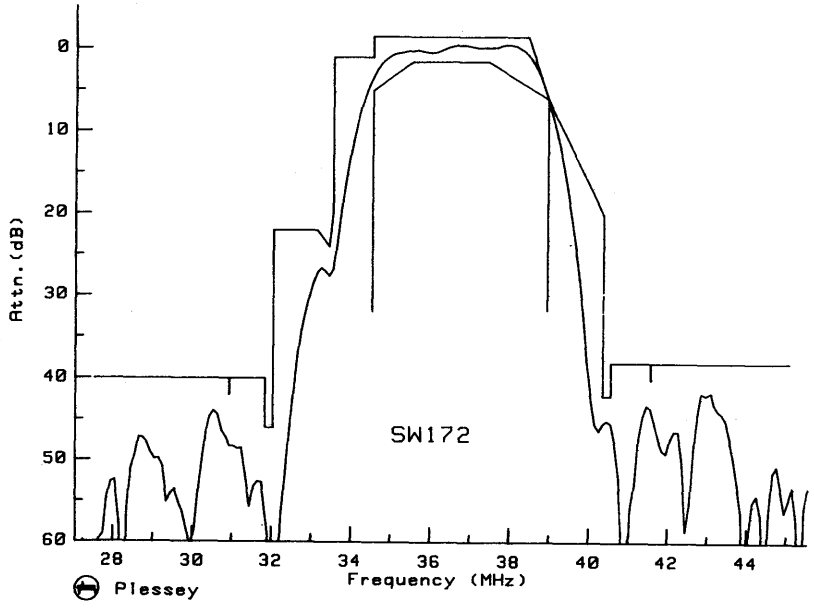
Characteristic	Frequency MHz	Value Min.	Value Typ.	Value Max.	Units	Conditions
Vision carrier	38.9		Ref. level −6		dB	
Colour carrier	34.47	−6	−3	0	dB	
Sound carrier	32.9	−25	−22	−19	dB	
In-band level	35.5–37.4	−2.5	0	2.5	dB	
In-band ripple	35.5–37.4		0.5	1.5	dB	Peak
Adjacent vision trap	30.9	−40	−46		dB	
Adjacent sound trap	40.9	−38	−43		dB	
Lower side lobe	25.8–30.9	−38	−45		dB	
Upper side lobe	40.9–46	−35	−40		dB	
Insertion loss		18	20	24	dB	
2T sin² pulse and bar K rating	38.9		1.5	2	%	
Group delay deviation	35.5–37.4		25	50	ns	
Spurious outputs	38.9		−46	−40	dB	
Temperature coefficient of frequency			−72		ppm/°C	
Small signal impedances						
Input pins 2 & 4			1.6kΩ// 8pF			
Output pins 1 & 5			1.8kΩ// 10pF			

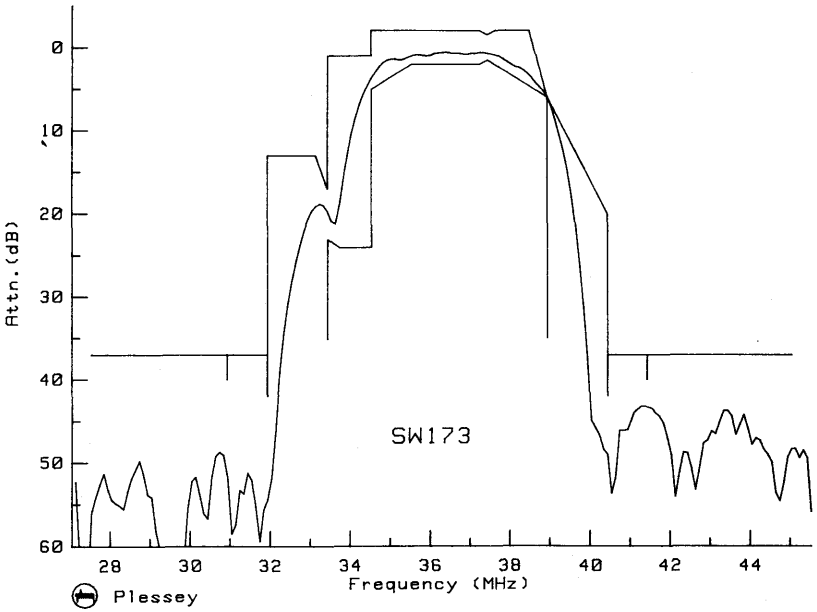
ABSOLUTE MAXIMUM RATINGS

Storage temperature	−25°C to +85°C
Operating temperature	−10°C to +70°C
Pin to pin voltage	30V (short term)
	10V (continuous)
Pin to case voltage	100V

TYPICAL AMPLITUDE RESPONSES






0
10
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Attn.(dB)
SW173
28
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32
34
36
38
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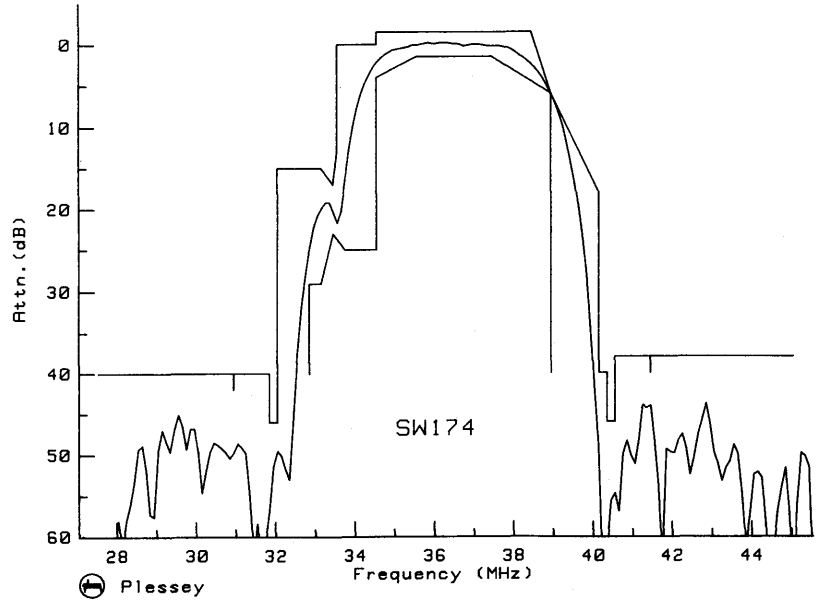
42
44
Frequency (MHz)
Plessey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Attn.(dB)
SW174
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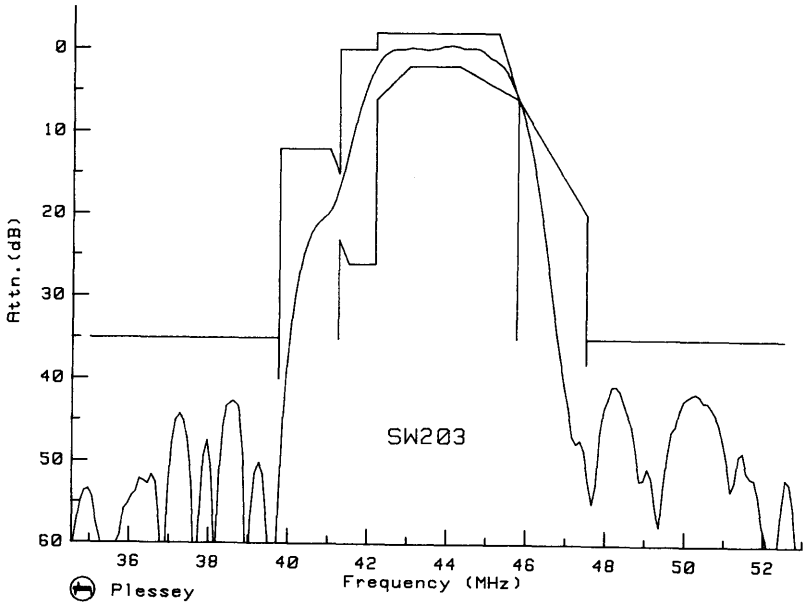
Frequency (MHz)
Plessey


Attn.(dB)
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SW203
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38
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42
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46
48
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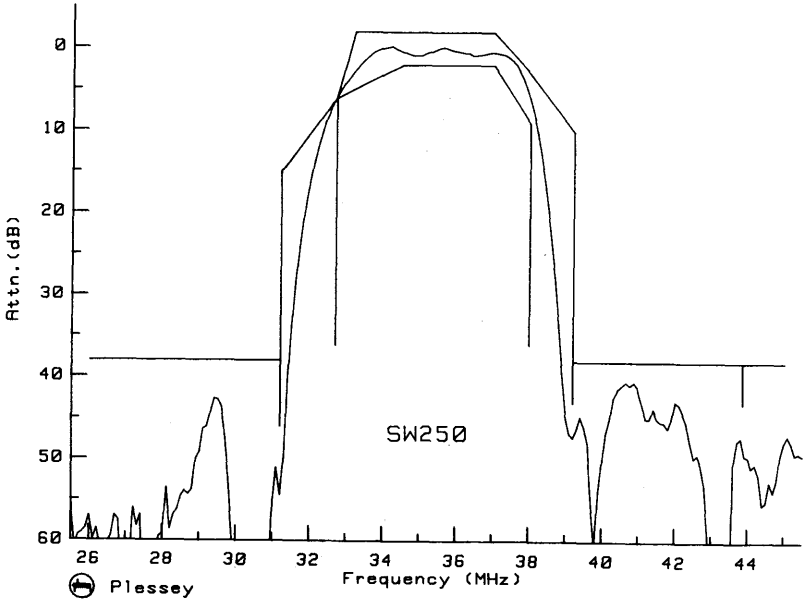
52
Frequency (MHz)
Plessey


Attn.(dB)
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20
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SW250
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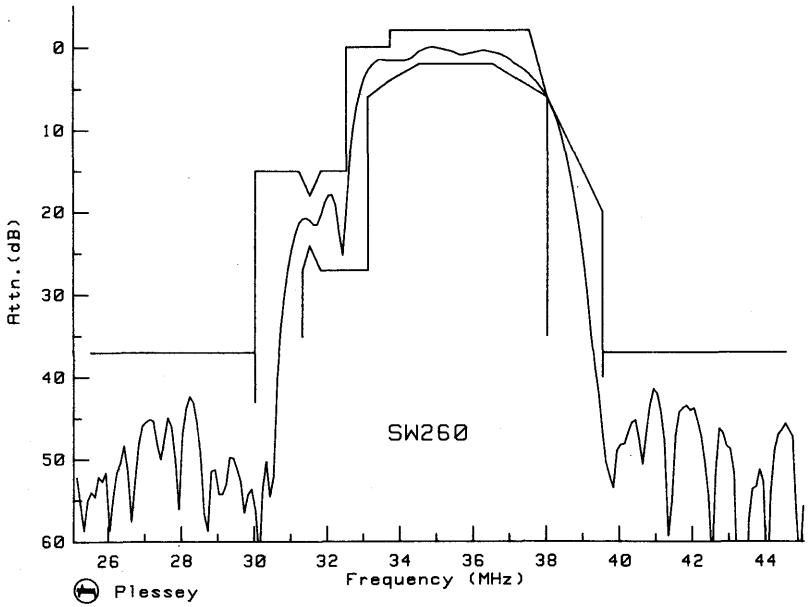
28
30
32
34
36
38
40
42
44
Frequency (MHz)
Plessey


Attn.(dB)
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10
20
30
40
50
60
SW260
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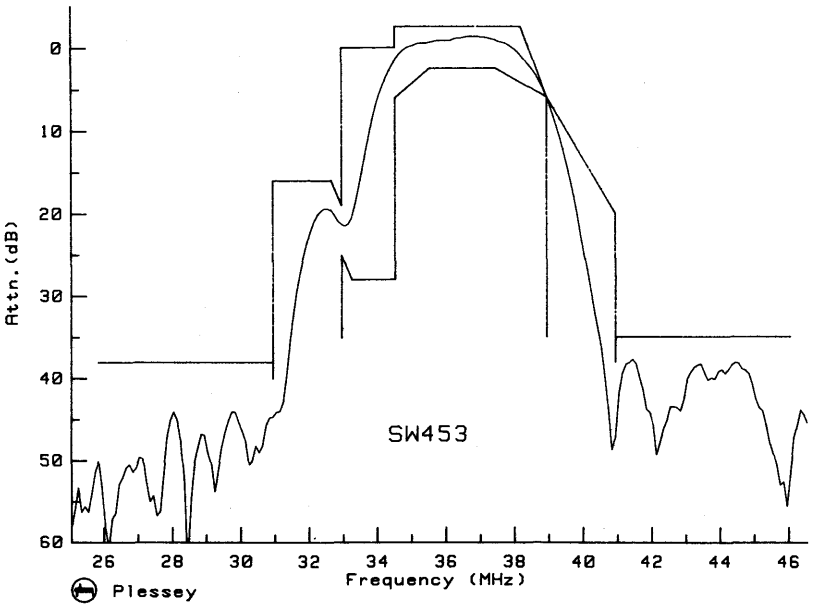
28
30
32
34
36
38
40
42
44
Frequency (MHz)
Plessey


Attn.(dB)
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10
20
30
40
50
60
SW453
26
28
30
32
34
36
38
40
42
44
46
Frequency (MHz)
Plessey

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ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

SW185

SURFACE ACOUSTIC WAVE COLOUR TV IF FILTER FOR PARALLEL SOUND

The SW185 is one of a range of surface acoustic wave IF filters for use with TV parallel sound. It has been optimised for systems B & G with a vision carrier of 38.9MHz. There are two balanced outputs for vision and sound signal processing. The vision output has a very low level of sound carrier, and the sound output has two broad peaks at the sound and vision carriers with rejection between them.

The device is optimised for use with a new range of parallel sound circuits from Plessey Semiconductors, initially coded XL, for example XL1441.

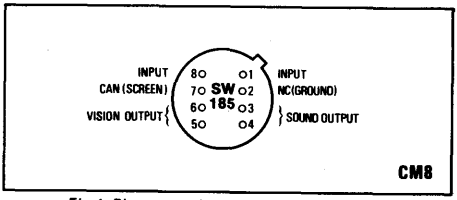


Fig.1 Pin connections (viewed from beneath)

FEATURES

- No Adjustment Necessary
- Compact Dimensions
- High Stability and Reliability
- Elimination of Sound Chroma Interference
- Improved Sound Quality
- Stereo Sound Compatible

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Ambient temperature	+35°C
Input drive impedance	50Ω
Load impedance	250Ω balanced

(Refer to SW153/453 data sheet for definition of terms)

SW185 SOUND CHANNEL

Characteristic	Frequency MHz	Value			Units	Conditions
		Min.	Typ.	Max.		
Vision Carrier	38.9		Ref. level 0		dB	
	38.7 to 39.1	-2		1	dB	
Sound Carrier	33.4	-2	1	4	dB	
Sound Shelf	32.8 to 33.8	-5		1	dB	wrt level at 33.4MHz
In-band trap	35 to 37.4	-10	-16		dB	
Adjacent vision trap	31.9	-30	-38		dB	
Adjacent sound trap	40.1 to 40.3	-30	-38		dB	
	40.3 to 40.5	-32	-42		dB	
Lower side lobe	27.5 to 31.9	-26	-32		dB	
Upper side lobe	40.4 to 45	-30	-35		dB	
	45 to 100		-20			
Insertion loss	38.9		28	32	dB	
2Tsin² pulse and bar K rating						
Group delay deviation	32.8 to 39.1		50	100	ns	
Temperature Coefficient of frequency			-90		ppm/°C	

SW185 VISION CHANNEL

Characteristic	Frequency MHz	Value			Units	Conditions
		Min.	Typ.	Max.		
Vision Carrier	38.9		Ref. level -6		dB	
Colour Carrier	34.5	-6	-4	-2	dB	
Sound Carrier region	32 to 33.5	-30	-40		dB	
In-band level	35.5 to 37.4	-2	0	2	dB	
In-band ripple	35.5 to 37.4		0.5	1	dB	Peak
Adjacent vision trap						
UHF	30.9	-40	-48		dB	
VHF	31.8 to 32	-42	-50		dB	
Adjacent sound trap						
VHF	40.1 to 40.3	-40	-46		dB	
	40.3 to 40.5	-42	-50		dB	
UHF	41.4	-40	-44		dB	
Lower side lobe	27.5 to 31.9	-37	-42		dB	
Upper side lobe	40.4 to 45	-37	-42		dB	
	45 to 100		-30		dB	
Insertion loss			22	26	dB	Measured at 38.9MHz as a voltage ratio and corrected by 6dB to relate to 0dB in-band level.
2Tsin² pulse and bar K rating			2	3	%	
Group delay deviation	34.1		80		ns	
	34.5	40	60	80	ns	
	35.15		0		ns	
	36.9		-90		ns	
	37.9		-55		ns	
	39.9		-20		ns	
Spurious outputs	38.9		-48	-42	dB	
Temperature Coefficient of frequency			-90		ppm/°C	

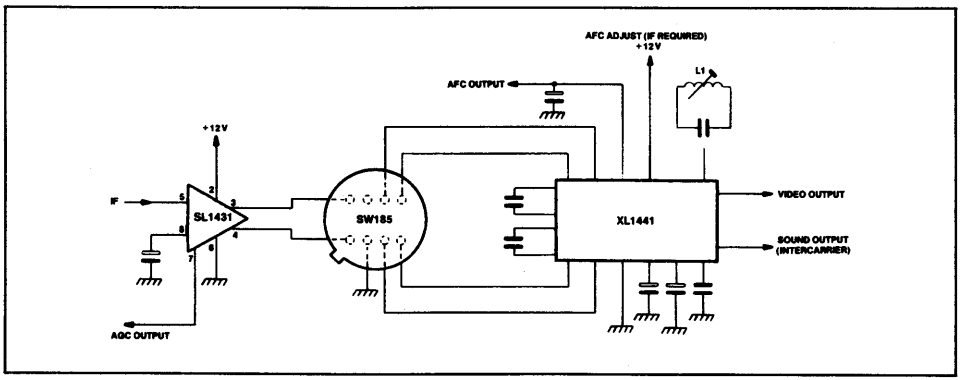


Fig.2 Typical application

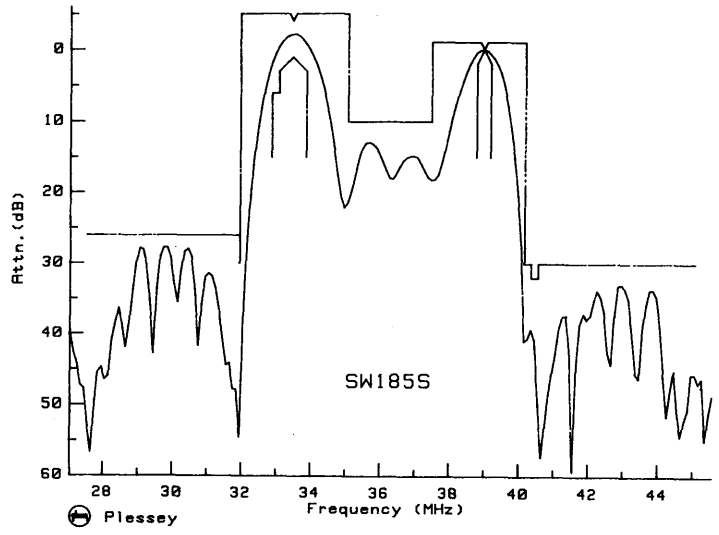


Fig.3 Typical amplitude response of vision output

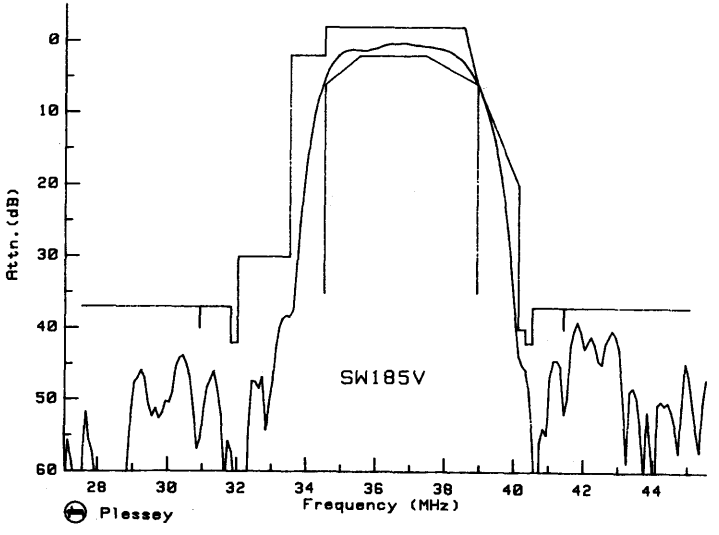


Fig.4 Typical response of sound output

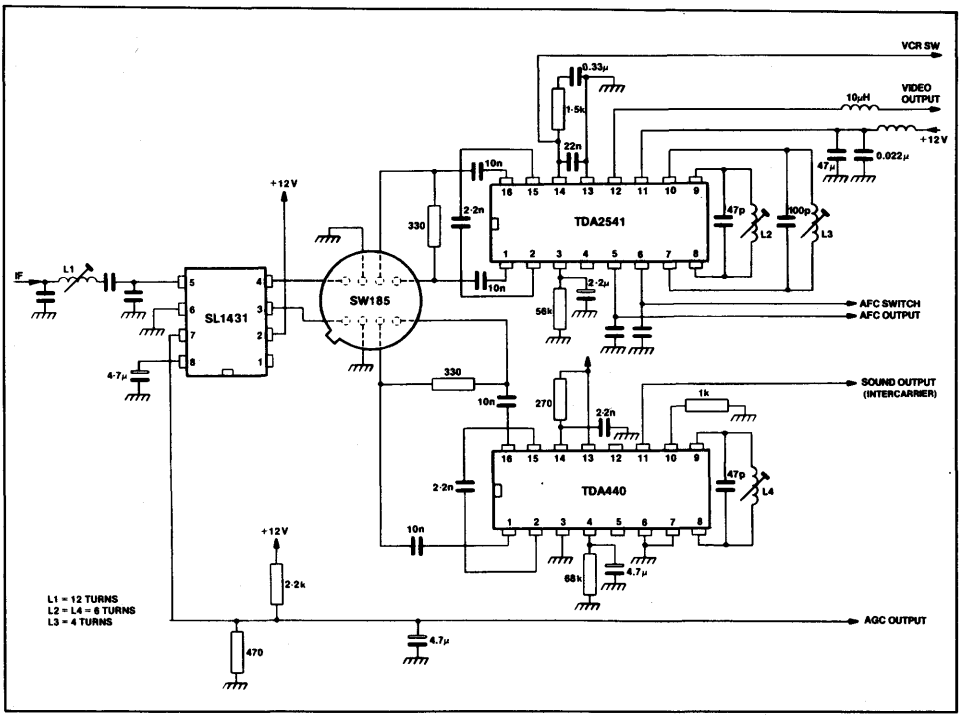


Fig.5 Application with TDA440 and TDA2541

PLESSEY
Semiconductors

TBA120S

LIMITING IF AMPLIFIER/FM DETECTOR

The TBA120S is a symmetrical 8-stage limiting amplifier with a symmetrical coincidence demodulator and remote DC volume control. The circuit is especially suited for the sound IF section of TV receivers and for FM/IF amplification/demodulation in FM radio receivers.

An auxiliary circuit, consisting of a transistor with free base and collector and a 12V Zener diode, is also incorporated on the chip. The transistor can be used as an AF preamplifier (I_C<5mA) or as a bass/treble switch using voltage-controlled on/off switching of an R-C circuit.

The Zener diode can be used to stabilize the chip supply voltage or that of other circuits in the system (I_Z<15mA).

The TBA120S is supplied in two group variants, with volume as the parameter. A decrease in volume of 30 dB requires a resistor between pin 5 and earth with a value depending on the group number as shown in the following table. The group number is printed on the package.

Group	III	IV
R_5(kΩ)	2.1–2.5	2.4–2.9

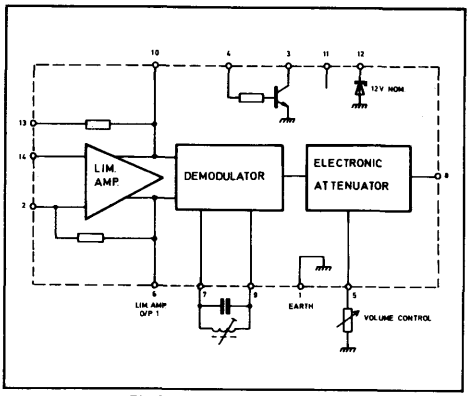


Fig.2 TBA120S block diagram

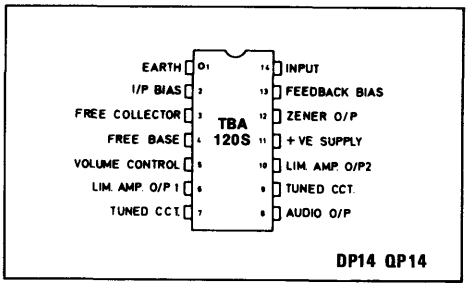


Fig. 1 Pin connections

FEATURES

- Outstanding Limiting Qualities
- High AM Suppression
- Wide Supply Voltage Range
- Low External Component Count

APPLICATIONS

- TV Sound Systems
- FM Radio Receivers
- FM Tuners

QUICK REFERENCE DATA

- Supply Voltage: +12V (Typ.)
- Operating Frequency: Up to 12MHz
- Current Consumption: 14mA (Typ.)
- IF Voltage Gain: 68dB (Typ.)
- AF Output Voltage: 1.1V r.m.s. (Typ.)
- Volume Control Range: 70dB (Typ.)
- Second Source Availability

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

V_{CC} = +12V
T_A = +25°C
f = 5.5MHz
Δf = ±50kHz
f_{mod} = 1kHz

Characteristics	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Amplifier/demodulator						
Frequency range	f	0		12	MHz	
IF voltage gain V_6/V_{14}	G_V		68		dB	
IF output voltage	V_{opp}		250		mV	Limiting each output
AF output voltage	V_{AF}		1.1		V r.m.s.	V_i=10mV, Q=45, K=4%
			0.55		V r.m.s.	V_i=10mV, Q=20, K=1%
Input voltage at start of limiting	V_{lim}		30	60	μV	Q=45
Input impedance	Z_i	15/6	40/4.5		kΩ/pF	
Output resistance (pin 8)	R_O		2.6		kΩ	
Volume control range	$\frac{V_{AF\ max}}{V_{AF\ min}}$		70		dB	
DC component of o/p signal	V_8		7.3		V	V_i=0
AM suppression	a_{AM}	45	55		dB	V_i=500μV, m=30%
Potentionmeter resistance	R_5					
−1dB down			3.7	4.7	kΩ	
−70dB down		1.0	1.4		kΩ	
Control voltage	V_5					
−1dB down			2.4	2.6	V	
−70dB down			1.3		V	
Total current requirement	I_{cc}	10	14	18	mA	$R_5 = \infty$
		12	16	20	mA	R_5 = 0
Auxiliary circuit						
Zener voltage	V_{12}	12.5	13.5	14.5	V	I_{12} = 5mA
Zener resistance	R_z		30		Ω	
Transistor breakdown voltage	BV_{CEO}	13			V	I_4=0, I_3=500μA
Current gain	h_{FE}	30			–	I_3=1mA

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}:	18V
Operating temperature	−10°C to +70°C
Storage temperature	−25°C to +125°C
Total power dissipation, P_{tot}	
Continous:	400mW
Max. 1 min:	500mW

Zener current, I_{12}	
Continuous:	15mA
Max. 1 min:	20mA
Volume control voltage, V_5:	4V
Collector current, I_3:	5mA
Current I_4:	2mA
Shunt resistance $R_{13/14}$:	⩽ 1kΩ

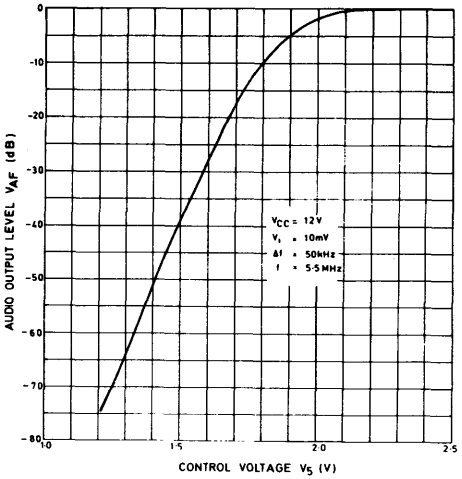


Fig. 3 Volume control voltage characteristic

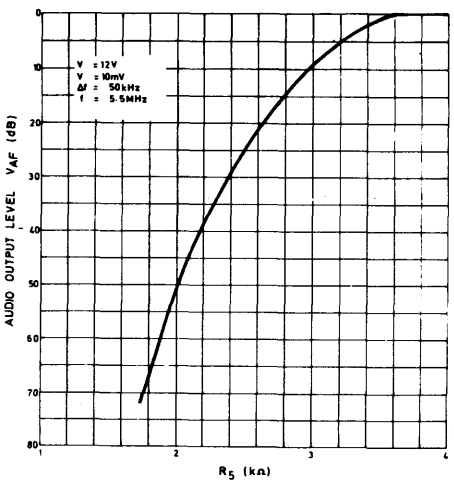


Fig. 4 Volume control resistance characteristic

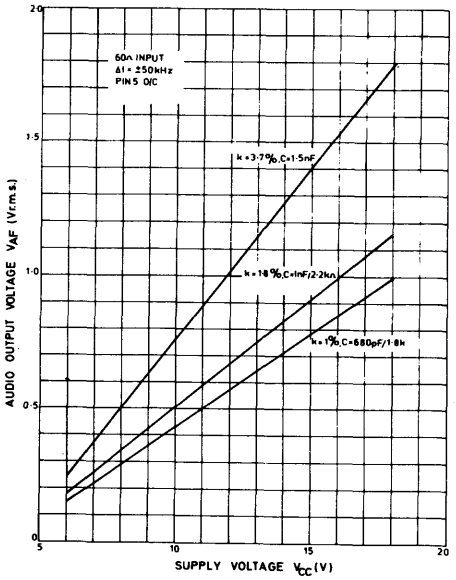


Fig. 5 Audio output v. supply voltage

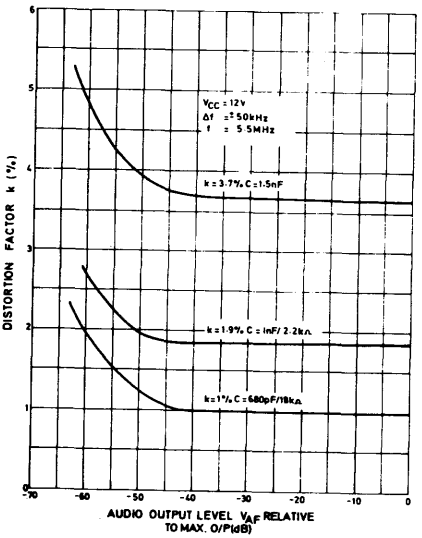


Fig. 6 Distortion factor (k) as a function of audio output voltage V_{AF}

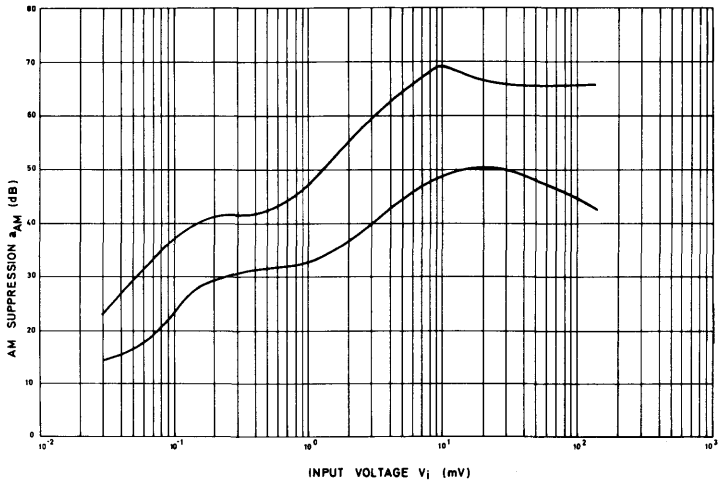


Fig. 7 AM suppression characteristics

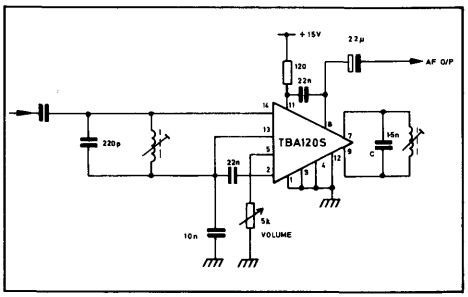
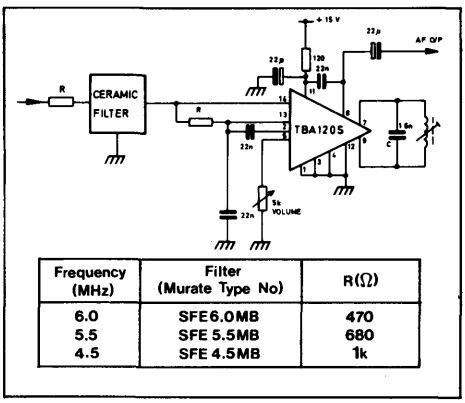


Fig. 8 Recommended application circuit, 5.5MHz



Frequency (MHz)	Filter (Murate Type No)	R(Ω)
6.0	SFE6.0MB	470
5.5	SFE 5.5MB	680
4.5	SFE 4.5MB	1k

Fig. 9 Application circuit using ceramic filter. (For good selectivity, the ceramic filter should be combined with an LC circuit.) ▷

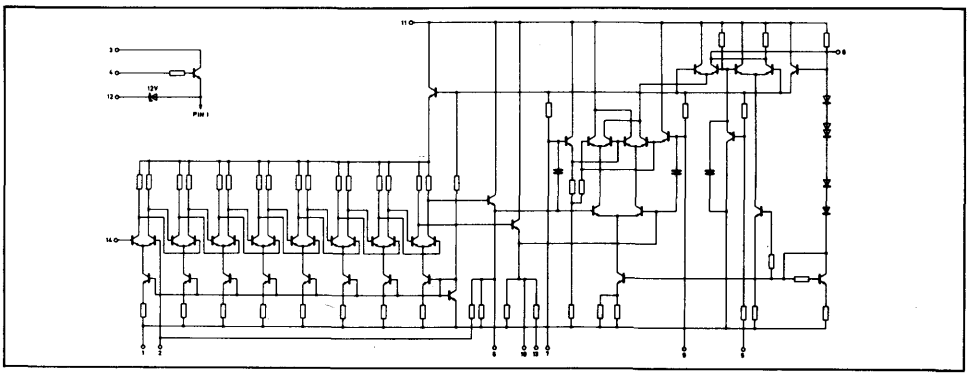


Fig. 10 Circuit diagram

PLESSEY
Semiconductors

TBA 120T TBA 120U

FM IF AMPLIFIER AND DEMODULATOR

The TBA120T and TBA120U are symmetrical 8-stage limiting amplifiers with symmetrical coincidence demodulator and remote DC volume control. The circuits are especially suitable for the sound IF section of TV receivers and for FM/IF amplification/demodulation in FM radio receivers. An additional audio output is provided at constant level (before the volume control) for the connection of video recorders and headphones, together with an audio input for video recorder playback.

The audio output voltage is at constant level with supply voltages between 10 and 18V and is of the same level as the TBA120S operating from a 15V supply.

The devices are insensitive to supply voltage hum, and there is therefore little need for smoothing capacitors.

FEATURES

- Outstanding Limiting Qualitites
- High AM Suppression
- Wide Supply Voltage Range
- Low External Component Count
- Low Intermodulation due to IF Voltage
- No Selection for Volume Control Characteristic Necessary
- Designed for use with Ceramic Filters (TBA120T only)

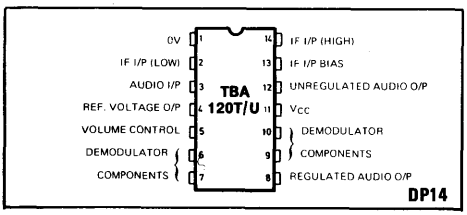


Fig. 1 Pin connections

APPLICATIONS

- TV Sound Systems
- FM Radio Receivers
- FM Tuners

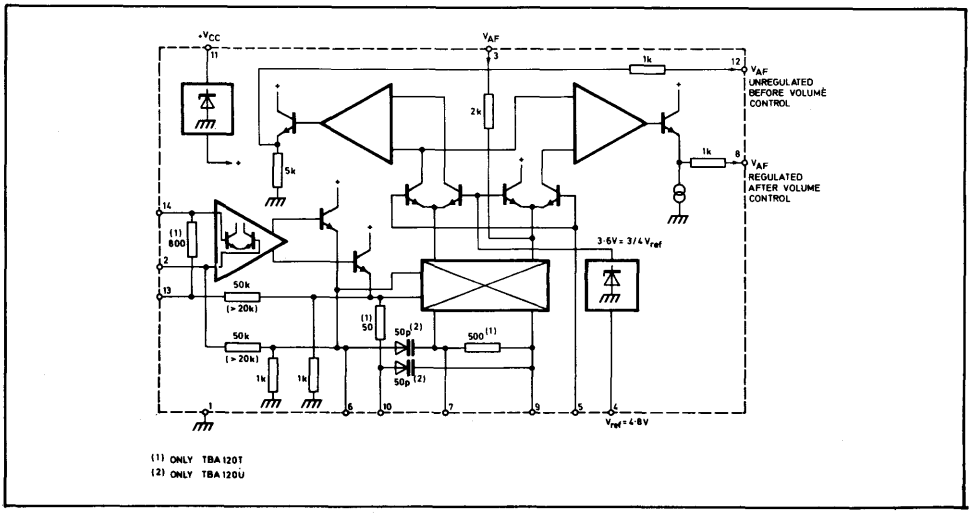


Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS

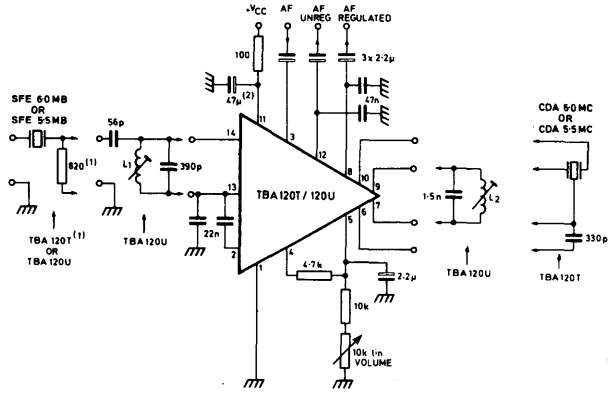
Test conditions (unless otherwise stated):
V_{CC} = 12V
T_{amb} = +25°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Total current consumption	I_{CC}	9.5	13.5	17.5	mA	
IF voltage gain V_6/V_{14}	G_V		68		dB	f_{IF} = 5.5 MHz
Output voltage with limiting at each output			250		mVp-p	
Output impedance Pin 8	R_8		1.1		kΩ	
Pin 12	R_{12}		1.1		kΩ	
Input impedance	R_3		2		kΩ	
Internal impedance	R_4		12		Ω	
DC level of output signal (V_{in} = 0)	V_8		4		V	V_{in} = 0
	V_{12}		5.6		V	
Stabilized voltage	V_4	4.2	4.8	5.3	V	
Residual IF voltage without deemphasis	V_8		20		mV	
	V_{12}		30		mV	
AF gain (AF not regulated)	V_8/V_3		7.5			
Regulation at certain ratio of divider	$V_{AF}/_8$	20	28	36	dB	R_{4-5} = 5kΩ, R_{5-1} = 13kΩ
Range of volume control (referred to pin 8)	$\frac{V_{AFmax}}{V_{AFmin}}$	70	85		dB	
Resistance (see note 1)	R_{4-5}	1		10	kΩ	
Input voltage for limitation	V_{inlim}		30	60	μV	f_{IF} = 5.5 MHz, Δf = ± 50kHz, f_{mod} = 1kHz
Hum suppression	V_8/V_{11}		35		dB	
	V_{12}/V_{11}		30		dB	
TBA 120T only:						
Input impedance	Z_{in}		800//5		Ω//pF	f_{IF} = 5.5 Mhz
AM suppression	a_{AM}	50	60		dB	f_{IF} = 5.5 MHz, Δf = ±50kHz, V_{in} = 500μV, f_{mod} = 1kHz, m = 30%
AF output voltage	V_8	650	900		mV	f_{IF} = 5.5 MHz, Δf = ±50kHz,
	V_{12}	400	650		mV	f_{mod} = 1kHz
TBA 120U only:						
Input impedance	Z_{in}	15//6	40//4.5		kΩ//pf	f_{IF} = 5.5 MHz
AM suppression	a_{AM}	50	60		dB	f_{IF} = 5.5 MHz, Δf = ±50kHz, V_{in} = 500μV, f_{mod} = 1kHz, m = 30%
AF output voltage	V_{8eff}	850	1200		mV	f_{IF} = 5.5 MHz, Δf = ±50kHz, V_{in} = 500μV, f_{mod} = 1kHz,
	V_{12eff}	600	1000		mV	$Q_8 \approx 45$, k = 4%
Harmonic distortion	k		1		%	f_{IF} = 5.5 MHz, Δf = ±50kHz, V_{in} = 10mV, f_{mod} = 1kHz, $Q_8 \approx 20$

NOTE
1. If DC volume control is not used, pin 4 must be connected direct to pin 5.

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	18V	Reference voltage O/P current, I_4	5mA
Operating ambient temperature, T_{amb}	−10 to +65°C	IF input resistance, R_{13-14} (TBA120U)	⩽ 1kΩ
Storage temperature, T_{stg}	−55 to +125°C	Range of supply operation, V_{CC}	10 to 18V
Total power dissipation, P_{tot}	400mW	Frequency range, f	0 to 12 MHz
Volume control voltage, V_5	6V		



NOTES
1. This 820Ω resistor is not necessary for the TBA120T, when using the SFE 5.5MB
2. Omitting the 47µF capacitor on pin 11 changes volume control range
3. L1: $Q_0 \approx 73$
4. L2: $Q_0 \approx 40$

Fig. 3 Recommended application circuit

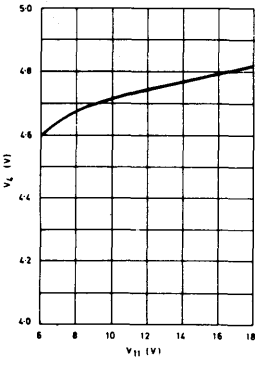


Fig. 4 Z voltage v. supply voltage

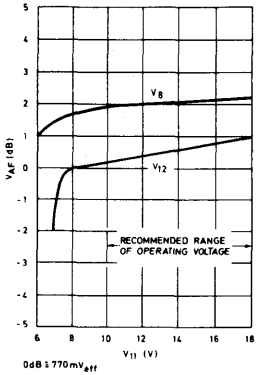


Fig. 5 AF output voltage v. supply voltage

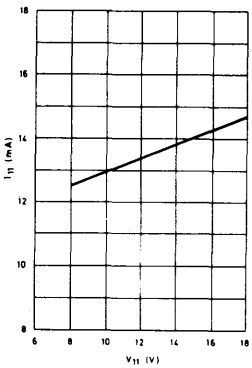


Fig. 6 Total current consumption v. supply voltage

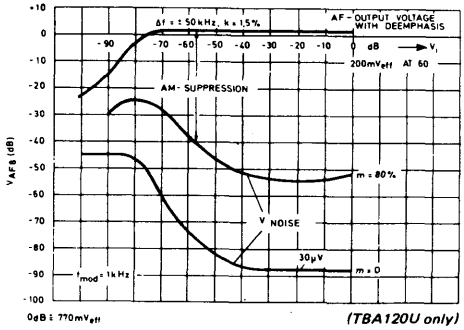


Fig. 7 AF output voltage and noise voltage v. input voltage (input Murata SFE 5.5MB)

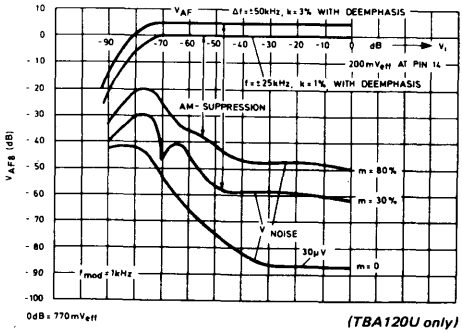


Fig. 8 AF output voltage and noise voltage v. input voltage (input 60Ω impedance, broadband)

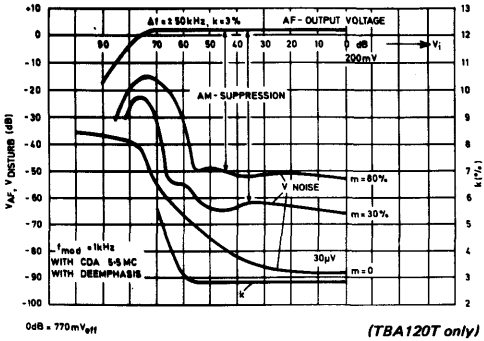


Fig. 9 AF output voltage (pin 8), noise voltage and harmonic distortion v. input voltage.

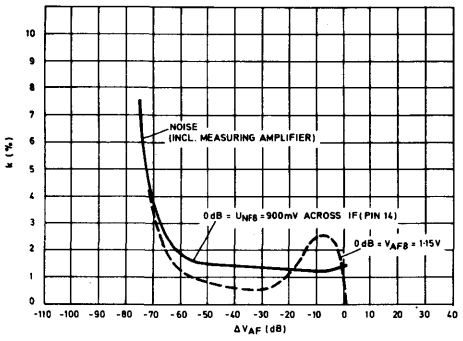


Fig. 10 Harmonic distortion v. volume control

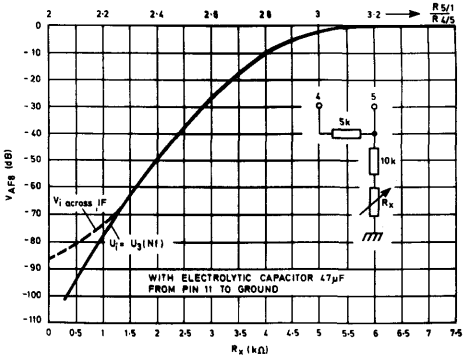


Fig. 11 AF output voltage (pin 8) v. potentiometer resistance and v. ratio of resistances

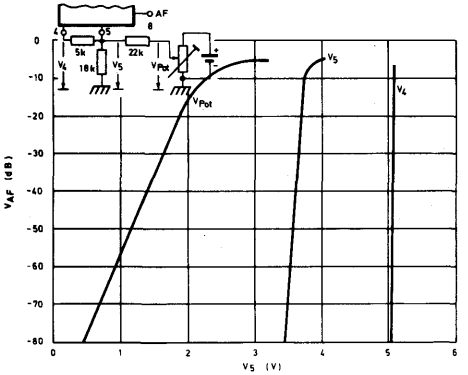
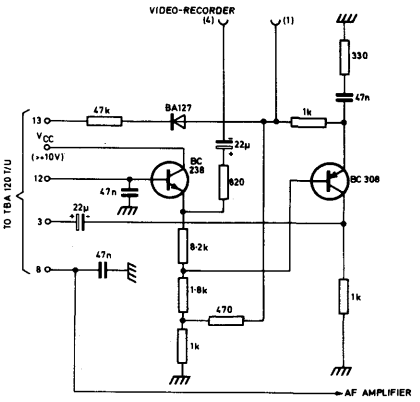


Fig. 12 AF output voltage (pin 8) v. voltage feeding into pin 5 V_{IRF} = 60mV$_{eff}$, f_{IF} = 5.5 MHz, Δf = ±50kHz, f_{mod} = 1kHz, V_{CC} = 18V



Function:

When switching voltage applied, the emitter follower (BC238) on the output is blocked and the buffer stage (BC308) is switched on. It includes a pre-emphasis to balance the de-emphasis at the AF output. The IF amplifier is put out of operation by the diode, BA127, and the 47kΩ resistor. The remote controllable volume regulator in the TBA120T/U is used for recording and playback.

SOCKET (1): SWITCHING VOLTAGE: FOR PLAYBACK +12V
FOR INPUT NC
SOCKET (4) SIMULTANEOUS INPUT AND OUTPUT FOR AF

Fig. 13 Circuit for direct connection to video recorders

PLESSEY
Semiconductors

TBA 440 N/P

VIDEO IF AMPLIFIER DEMODULATOR

The TBA440 (TBA440N for NPN tuners, TBA440P for PNP tuners) comprises a high-gain regulated video IF amplifier, a controlled demodulator and two low-resistance video outputs with positive and negative signal as well as the complete key control and delayed tuner control.

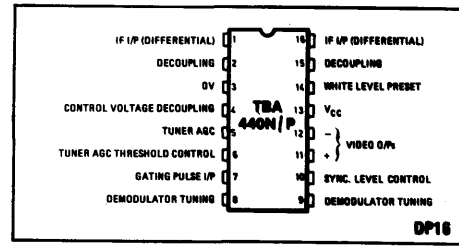


Fig. 1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Supply voltage steady	15V
transitory	16.5V
Voltage at pin 5	20V
Voltage at pin 4	5V
Voltage at pin 14	5V
Operating ambient temperature	−10° to +60°C
Total power dissipation at $T_{amb} \leqslant 55°C$	700mW
Ohmic resistance between pins 8 and 9	20Ω

FEATURES

- Complete Video IF in one IC
- High Sensitivity
- Positive and Negative Video Signals
- Gated AGC and Delayed AGC for Tuner
- White and Black Levels Separately Adjustable
- Ability to Control PIN Diode Attenuators

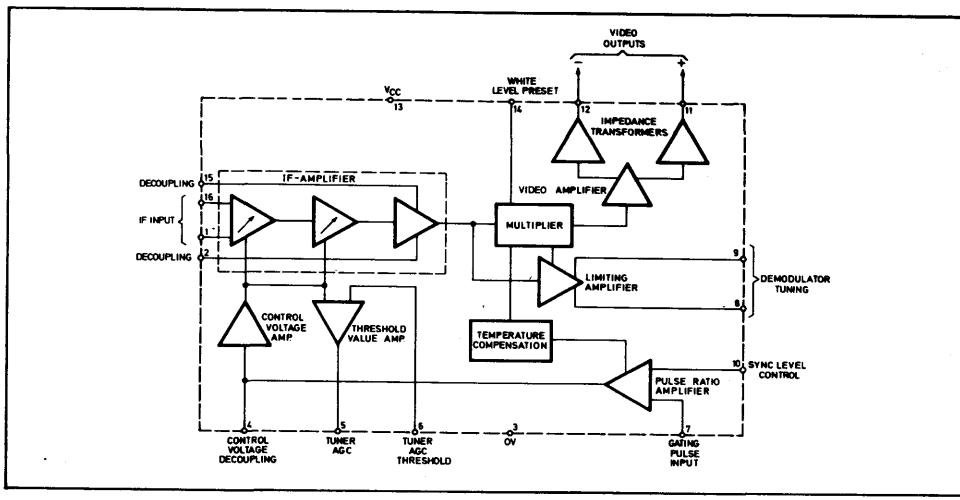


Fig. 2 TBA440 block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = +25°C
V_{CC} = +13V
Reference point is pin 3 (0V)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage, V_{CC}	13	10.5	13	15	V	
Current consumption	13	28	40	52	mA	V_{CC} = 15V
DC output voltage	11	4.1	5.1	6.1	V	V_{in} = 0V, $R_{14} = \infty$
	11		6.2		V	V_{in} = 0V, R_{14} = 0
	12	0 5	1.1	1.8	V	V_{in} = 0V, $R_{14} = \infty$
	12		2.5		V	V_{in} = 0V, R_{14} = 0
White level deviation						
$\Delta V_{11}/\Delta V_{13}$	11, 13		0.15			
$\Delta V_{12}/\Delta V_{13}$	12, 13		0.05			
Resistance R_{14-3} for ΔV_{11} = 1V	14 3		1		kΩ	
AGC threshold V_{10} = sync pulse level for R_{10-11} = 0	10,11		1.2		V	$V_{10} = V_{11}$
Regulating slope R_{10-11}/V_{11}	10, 11		4.5		kΩ/V	
Sync. pulse level with async. or without gating pulses	11		0.2		V	
Control current for tuner pre amp.	5	10	15		mA	$V_5 > 2V$, 10dB after AGC (TBA440P) 10dB before AGC (TBA440N)
IF control voltage for max gain	4	0		0.5	V	
for min gain	4	2.5		5	V	
Gating pulse voltage	7	−2		−5	V	
Residual IF voltage	11, 12		50		mV	
Output current to earth	11, 12			5	mA	
Output current to V_{13}	11, 12			−1	mA	
Input impedance at max gain	1		1.8//2		kΩ//pF	
at min gain	1		1.9//0		kΩ//pF	
Input voltage for V_{11} = 3V p-p	1		100		μV	Input 60Ω via 3:5 transformer
Video bandwidth			7		MHz	
AGC range		52	58		dB	
Intermodulation			55		dB	Input 0.3 to 1.5V p-p

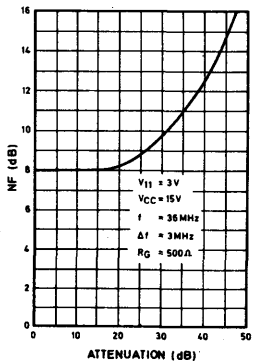


Fig. 3 Noise figure v. attenuation (measured at video frequency)

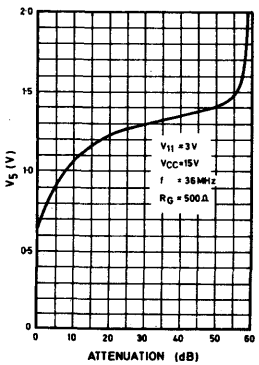


Fig. 4 Control voltage v. attenuation

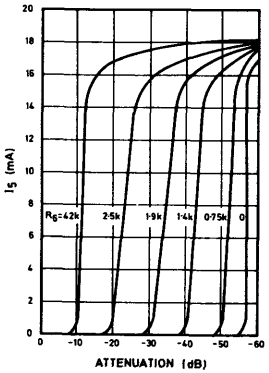


Fig. 5 Tuner control current v. attenuation with R_6 as parameter (TBA440P)

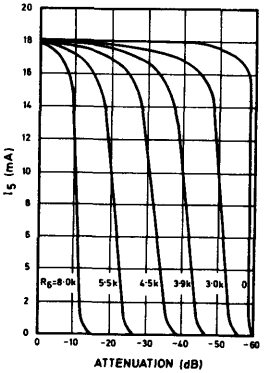


Fig. 6 Tuner control current v. attenuation with R_6 as parameter (TBA440N)

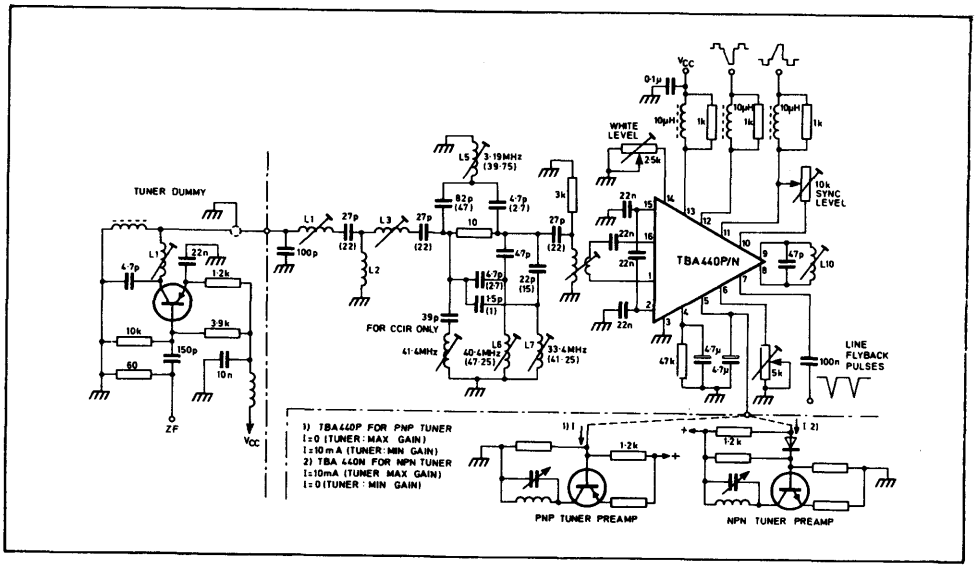


Fig. 7 IF application with TBA440P or TBA440N for CCIR standard (values in brackets for U.S. standard)

PLESSEY
Semiconductors

TBA530

RGB MATRIX PRE-AMPLIFIER

The TBA530 is an integrated R–G–B matrix pre-amplifier for colour television receivers incorporating a matrix pre-amplifier for R–G–B cathode or grid drive of the picture tube without clamping circuits. The chip layout has been designed to ensure tight thermal coupling between all transistors in each channel to minimise thermal drifts between channels. Also, each channel follows an identical layout to ensure equal frequency behaviour of the three channels.

This integrated circuit has been designed to be driven from the TBA520 synchronous demodulator integrated circuit.

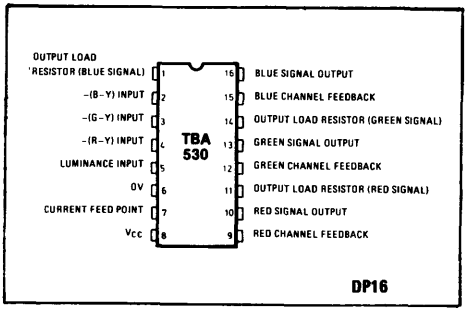


Fig. 1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	13.2V
Supply currents:–	
$I_1 = I_{11} = I_{14}$ max	10mA
$I_{10} = I_{13} = I_{16}$ max	50mA*
Total power dissipation at $T_{amb} = 60°C$, P_{TOT}	400mW*
Storage temperature	–55 to +125°C
Operating ambient temperature	–10 to +60°C

At increased voltages due to external failures (e.g., collector-base breakdown in the output transistors) a maximum current of 50mA is permitted between pins 16 and 8, 13 and 8, 10 and 8. The maximum permissible power dissipation is then 500mW.

QUICK REFERENCE DATA

- Supply Voltage (Nominal) 12V
- Total Supply Current (Nominal) 30mA
- Operating Ambient Temperature Range –10 to +60°C
- Gain of Luminance and Colour-difference Channels (Typ.) 100

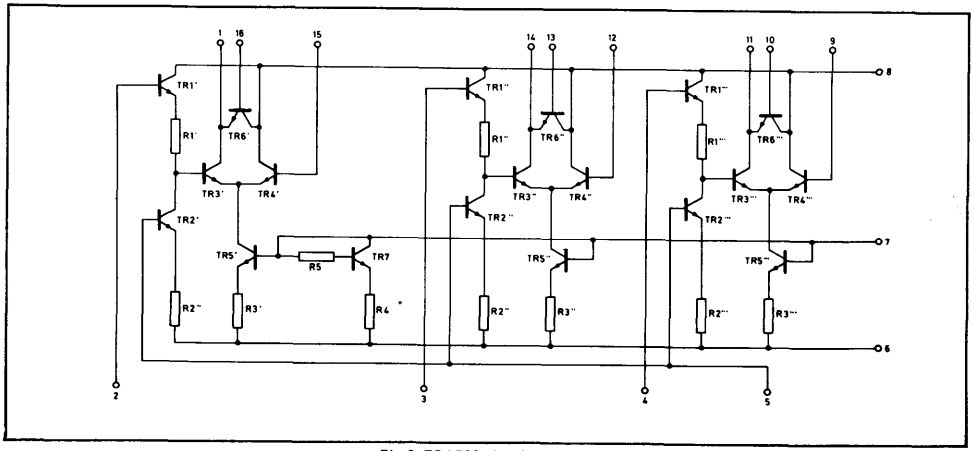


Fig.2 TBA530 circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):–
V_{CC} = +12V, T_{amb} = +25°C
Black level: $V_{R-Y} = V_{G-Y} = V_{B-Y}$ = 7.5V
V_Y = 1.5V
Reference = pin 6

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Gain of colour channels (B–Y, G–Y, R–Y)	G_2		100		–	
	G_3		100		–	f = 0.5MHz (see note 1)
	G_4		100		–	
Ratio of gain of luminance amplifier to colour amplifiers		0.9		1.1	–	
DC output voltages	V_R		140		V	
	V_G		140		V	See note 2
	V_B		140		V	
Input resistance of colour difference amplifiers	R_2		60		kΩ	
	R_3		60		kΩ	f = 1kHz
	R_4		60		kΩ	
Input capacitance of colour difference amplifiers	C_2		3		pF	
	C_3		3		pF	f = 1MHz
	C_4		3		pF	
Input resistance of luminance amplifier	R_5		20		kΩ	f = 1kHz
Input capacitance of luminance amplifier	C_5		10		pF	f = 1MHz
3dB bandwidth of all channels	B		6		MHz	
Total current drain	I_{TOT}		30		mA	

NOTES
1. *G is defined as the voltage ratio between the input signals at the pins 2, 3, 4 and the output signals at the collectors of the output transistors.*
2. At the collectors of the output transistors. The value of this voltage is also dependent on the external circuitry.

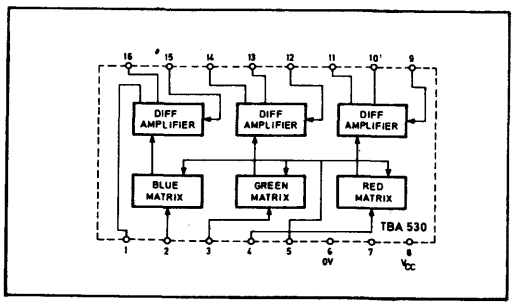


Fig.3 TBA530 block diagram

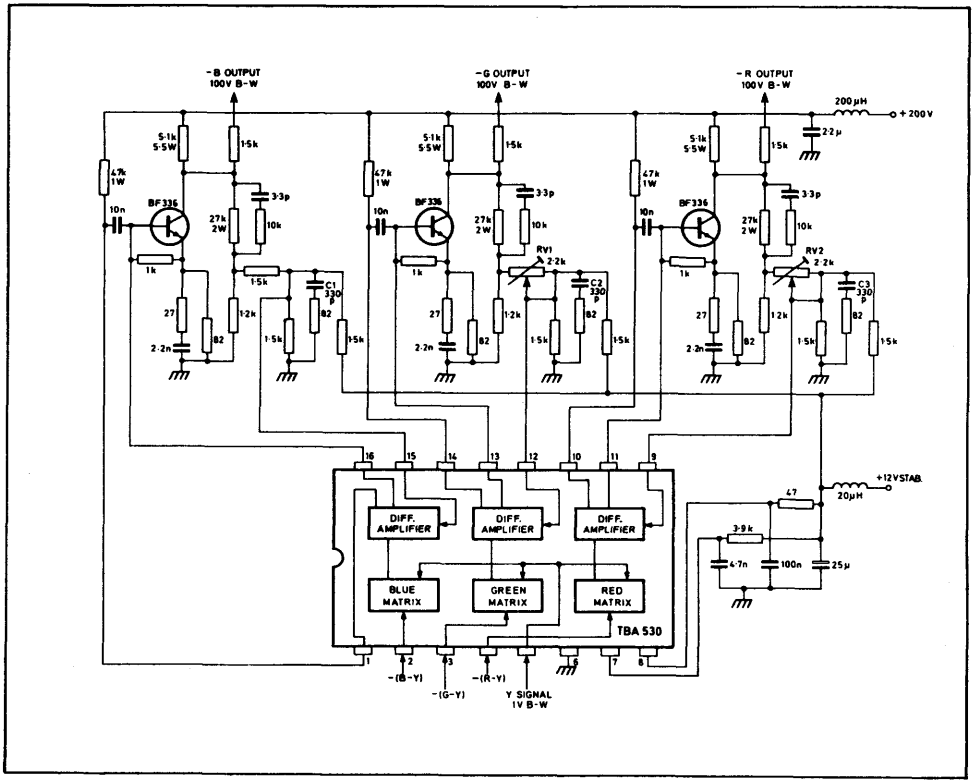


Fig. 4 Typical application diagram

FUNCTIONAL DESCRIPTION

Pin

1. Output load resistor, blue signal
   (Also pins 11 and 14 for red and green signals respectively.) Resistors (47kΩ, 1W) connected to +200V provide the high value loads for the internal amplifying stages. The nominal operating potential on these pins is defined by the IC and the DC feedback and is approximately +8V. The maximum current which can be allowed at each of these pins is 10mA.
2. −(B−Y) input signal
   This signal is fed via a low-pass filter from the TBA520 demodulator IC (pin 7) having a DC level of about +7.5V. The input resistance for this pin is typically 60kΩ with an input capacitance of less than 5pF (similarly for pins 3 and 4).
3. −(G−Y) input signal
   The DC black level of this signal is about +7.5V. (See pin 2.)
4. −(R−Y) input signal
   The DC black level of this signal is about +7.5V. (See pin 2.)
5. Luminance signal input
   The DC level on this pin for picture black is +1.6V. The required signal amplitude is 1V black-to-white with negative-going syncs (or blanking) for cathode drive as shown. The input resistance at this pin is 20kΩ approximately with a capacitance of less than 15pF.
6. Negative supply (earth).
7. Current feed point
   A current of approximately 2.5mA is required at this pin, fed via a 3.9kΩ resistor from +12V, to bias the internal differential amplifiers. A decoupling capacitor of 4.7nF is necessary.
8. Positive 12V supply
   Maximum supply voltage permitted, 13.2V. Current consumption approximately 30mA.
9. Red channel feedback (green channel, pin 12; blue channel, pin 15)
   The DC working points and gains of both the output stages and the IC amplifier stages are stabilised by the feedback circuits. The black level potentials at the collectors of the output stages (tube cut-off) are adjusted by setting correctly the DC levels of the colour difference signals produced by the TBA520 demodulator IC. The gains of the R−G−B output stages are adjusted to give the correct white points setting on the picture tube by adjusting the potentiometers in the feedback paths (RV1, RV2).
10. Red signal output (green and blue signal outputs on 13 and 16)
    These pins are internally connected with pins 11, 14 and 1 respectively via zener type junctions to give a DC level shift appropriate for driving the output transistor bases directly. To by-pass the Zener junctions at HF three 10nF capacitors are required.
11. Output load resistor, red channel (see pin 1).
12. Green channel feedback (see pin 9).
13. Green signal output (see pin 10).
14. Output load resistors, green channel (see pin 1).
15. Blue channel feedback (see pin 9).
16. Blue signal output (see pin 10).

OPERATING NOTES

Careful attention to earth paths should be given, avoiding common impedances between the input (decoder) side and the output stages. Also, to enable matched performance to be achieved, a symmetrical board and component layout should be adopted for the three output stages. To compensate for the effect upon HF response of inevitable differences the compensating capacitors C_1 and C_2 and C_3 may be appropriately selected for any given board layout.

The signal black level at the collectors of the R−G−B output stages depends upon the +12V supply, the DC level of the colour difference signals from the TBA520 demodulator IC and the black level potential of the luminance signal applied to the TBA530 matrix IC. The DC levels of the signals produced and handled by the IC's are designed to have approximately proportional tracking with the 12V supply potential,

$$\text{i.e.,}\ \frac{\Delta V\ \text{(DC level, signal)}}{\Delta V_{12V}} \triangleq \frac{V_{nom}\ \text{(DC level, signal)}}{12}$$

To ensure that changes in picture black level due to variations on the 12V supply to the IC's occur in a predictable way, all the IC's should be operated from a common supply line. This is specially important for the TBA520 and TBA530. Furthermore, to limit the changes in picture black level during receiver operation, the 12V supply should have a stability of not worse than ±3% due to operational variations.

To reduce the possibility of patterning on the picture due to radiation of the harmonics of the products of the demodulation process, the leads carrying the drive signals to the picture tube should be as short as the receiver layout will allow. Resistors (typically 1.5kΩ connected in series with the leads and mounted close to the collectors of the output transistors provide useful additional filtering of harmonics.

PLESSEY
Semiconductors

TBA 540

REFERENCE COMBINATION

The TBA540 is an integrated reference oscillator circuit for colour television receivers incorporating an automatic phase and amplitude controlled oscillator employing a quartz crystal, together with a half-line frequency synchronous demodulator circuit. The latter compares the phases and amplitude of the swinging burst ripple and the PAL flip-flop waveform, and generates appropriate ACC, colour killer and identification signals. The use of synchronous demodulation for these functions permits a high standard of noise immunity.

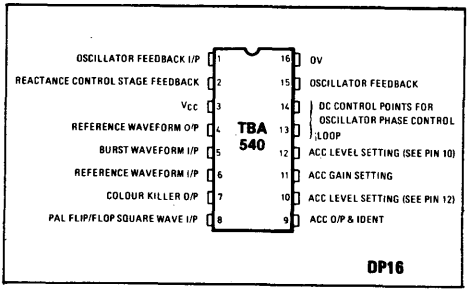


Fig. 1 Pin connections

QUICK REFERENCE DATA

- Supply Voltage, $V_{3\text{-}16}$: 12V (Nom.)
- Total Current Drain, I_3 : 38mA (Typ.)
- R-Y Ref. Output, $V_{4\text{-}16}$: 1.4Vpp (Typ.)
- Colour Killer Output, $V_{7\text{-}16}$
  Colour ON : 12V (Typ.)
  Colour OFF: 250mV (Max.)
- ACC Output Voltage, $V_{9\text{-}16}$:—
  at Correct Phase of PAL Switch : +0.2 to +4V
  at Incorrect Phase of PAL Switch : +4 to +11V

ABSOLUTE MAXIMUM RATINGS

Voltages are referred to pin 16

Electrical

Supply voltage V_3 (V_{CC})	13.2V
Total power dissipation at T_{amb} = +60°C	700 mW
Surge current, minimum duty cycle 10:1, I_{7max}	50mA

Temperature

Storage temperature, T_{stg}	−55°C to +125°C
Operating temperature, T_{amb}	−10°C to +60°C

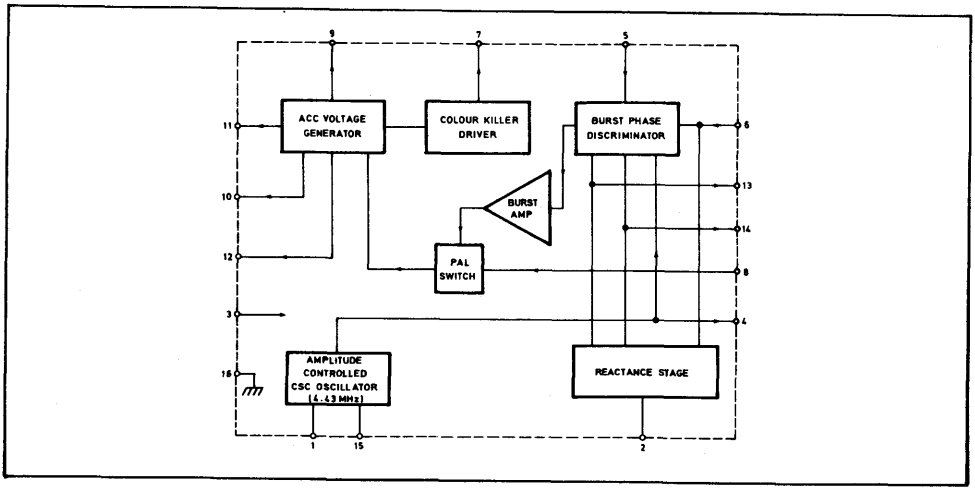


Fig. 2 TBA540 block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

V_{CC} (V_3) = +12V, T_{amb} = +25°C, V_5 = 1.5Vp-p burst, V_8 = 2.5Vp-p PAL square wave.
Voltages referred to pin 16

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Output Signals						
B-Y reference signal output	4	1	1.4	2	Vp-p	
Colour killer output	7					
colour 'on'			12		V	
colour 'off'			100	250	mV	
ACC output signal range	9					
at correct phase of PAL switch			+4 to +0.2		V	
at incorrect phase of PAL switch			+4 to +11		V	
Oscillator Section (Amplifier)						
Input resistance	15		3.5		kΩ	
Input capacitance	15		5		pF	
Voltage gain, $G_{15\text{-}1}$	15-1		4.7			
Reactance Control Section						
Voltage gain, $G_{15\text{-}2}$	15-2		1.3			Pins 13 and 14 interconnected
Rate of change of gain with phase difference between burst and reference signal, $\frac{\Delta G_{15\text{-}2}}{\Delta\phi 5\text{-}4}$	15-2		5		rad^{-1}	

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. Oscillator Feedback Output

The crystal receives its energy from this pin. The output impedance is approximately 2kΩ in parallel with 5pF.

2. Reactance Control Stage Feedback

This pin is fed internally with a sinewave derived from the reference output (pin 4) and controlled in amplitude by the internal reactance control circuit. The phase of the feedback from pin 2 to the crystal via C1 is such that the value of C1 is effectively increased. Pin 2 is held internally at a very low impedance therefore the tuning of the crystal is controlled automatically by the amplitude of the feedback waveform and its influence on the effective value of C1.

3. Positive 12V Supply

The maximum voltage must not exceed 13.2V.

4. Reference Waveform Output

This pin is driven internally by the regenerated subcarrier waveform in B-Y phase. (The output is in B-Y rather than R-Y phase as the burst phase network produces a lag of 90° of the burst applied to pin 5.) An output amplitude of nominally 1.4V peak-to-peak is produced at low impedance. No DC load to earth is required. A DC connection between pins 4 and 6 is, however, necessary via the bifilar coupling inductor. The function of this inductor is to produce, on pin 6, a signal of equal amplitude and opposite phase (-)B-Y)) to that on pin 4. A centre tap on the inductor, connected to earth via a DC blocking capacitor, is therefore necessary.

5. Burst Waveform Input

A burst waveform amplitude of 1.5V peak-to-peak is required to be AC coupled to this pin. The amplitude of the burst will normally be controlled by the adjustment and operation of the ACC circuit. The input impedance at this pin is approximately 1kΩ and a threshold level of 0.7V must be exceeded before the burst signal becomes effective. A DC bias of 400mV is internally derived for pin 5.

The absolute level of the tip of the burst at pin 5 will normally reach 1.5V.

6. Reference Waveform Input

This pin requires a reference waveform in the -(B-Y) phase, derived from pin 4 via a bifilar transformer (see pin 4), to drive the internal balanced reactance control stage. A DC connection between pins 4 and 6 must be made via the transformer.

7. Colour Killer Output

This pin is driven from the collector of an internal switching transistor and requires an external load resistor (typically 10kΩ) connected to +12V. The unkilled and killed voltages on this pin are then +12V and <250mV respectively. (The voltage range on pin 9 over which switching of the colour killed output on pin 7 occurs is nominally +2.5V.)

8. PAL Flip-Flop Square Wave Input

A 2.5V peak-to-peak square wave derived from the PAL flip-flop (in the TBA520 or TBA990 demodulator IC) is required at this pin, AC – coupled via a capacitor. The input impedance is about 3.3kΩ.

9. ACC Output

An emitter follower provides a low impedance output potential which is negative-going with a rising burst input amplitude. With zero burst input signal the DC potential produced at pin 9 is set to be +4V (RV1). The appearance of a burst signal on pin 5 will cause the potential on pin 9 to go in a negative direction in the event that the PAL flip-flop is identified to be in the correct phase. The range of potential over which full ACC control is exercised at pin 9 is determined by the control characteristic of the ACC amplifier, i.e., for the TBA560 from 0.8 to 1V. The potential on pin 9 will fall to a value within this range as the burst input signal is stabilised to an amplitude of 1.5V peak-to-peak. The latter condition is achieved by correct adjustment of RV2. If, however, the PAL flip-flop phase is wrong the potential on pin 9 will move positively. The potential divider R5, R6 will then operate a PAL switch cut-off function in the TBA520 demodulator IC.

10. ACC Level Setting

The network connected between pins 10 and 12 balances the ACC circuit and RV1 is adjusted to give +4V on pin 9 with no burst input signal to pin 5. C5 provides filtering.

11. ACC Gain Control

RV2 is adjusted to give the correct amplitude of burst signal on pin 5 (1.5V peak-to-peak) under ACC control.

12. See Pin 10.

13. See Pin 14.

14. DC Control Points in Reference Control Loop

Pins 13 and 14 are connected to opposite sides of a differential amplifier circuit and are brought out for the purpose of DC balancing of the reactance stage and the connection of the bandwidth-determining filter network. Two 2% tolerance 10k resistors with the addition of a 270Ω resistor at pin 13 are used in place of the previous balancing network. The 270Ω resistor may be modified according to the nature of the noise that appears at pin 5.

The filter network consists of R2, C2, C3 and C4. The DC potentials on these pins are nominally +6V.

15. Oscillator Feedback

The input impedance at this pin is nominally 3.5kΩ in parallel with 5pF. No DC connection is required on this pin. The voltage gain in the IC between pins 15 and 1 is nominally 4.7 times.

16. Negative Supply (earth).

OPERATING NOTES

Performance and Comments

Initial adjustment

(a) *Remove burst signal.*
(b) Short-circuit pins 13-14. Adjust oscillator to correct frequency by C1.
(c) Set the ACC level adjustment RV1, to give +4V on pin 9. Remove short circuit.
(d) Apply burst signal.
(e) Adjust ACC gain, RV2, to give a burst amplitude of 1.5V peak-to-peak on pin 5.

Phase lock loop performance (with crystal type 4322 152 0110)

(a) Phase difference between reference and burst signals for ±400Hz deviation of crystal frequency, ±10°.
(b) Typical holding range, ±600Hz. (c)
(c) Typical pull-in range ±300Hz.
(d) Temperature coefficient of oscillator frequency, only 2Hz/°C maximum.

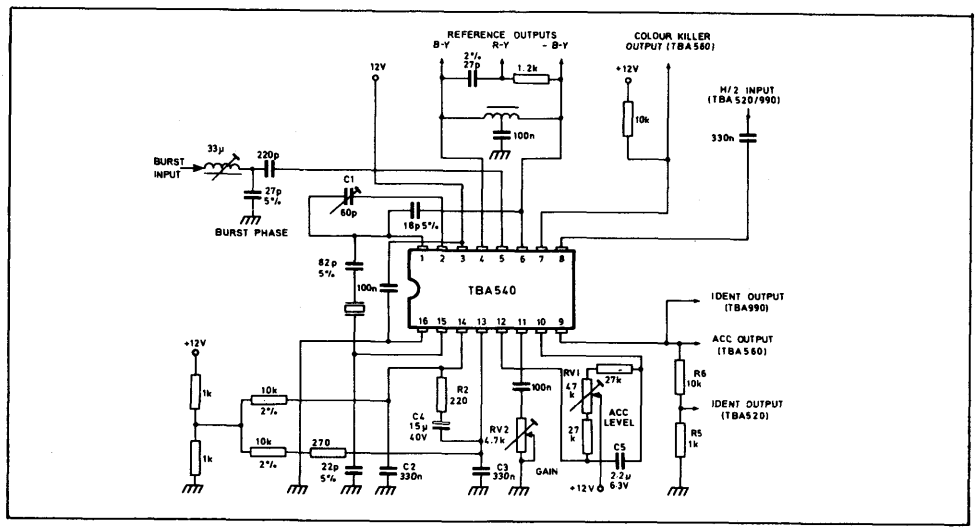


Fig. 3 Typical application diagram

PLESSEY
Semiconductors

TBA 560 C

LUMINANCE AND CHROMINANCE CONTROL COMBINATION

The TBA560C is an integrated circuit for colour television receivers incorporating circuits for the processing and control of the luminance and chrominance signals. It can be used in conjunction with the TBA520 or TBA990, 530, 540, 550 and TCA800 integrated circuits.

The luminance part provides luminance delay line matching, DC contrast control, black level clamp circuit, brightness control and flyback blanking.

The chrominance part provides chroma amplification with ACC, DC chroma gain control which tracks with the contrast control, separate saturation control, burst gate, chroma signal flyback blanking, colour killer and PAL delay line driver.

The TBA560C is not an equivalent of the TBA500 and 510 although it performs similar functions to those circuits.

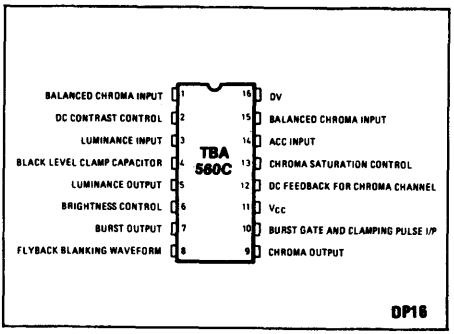


Fig. 1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Voltages are referred to pin 16

Electrical

V_{11} max.	Supply voltage (note 1)		13.2V
V_1	0 to +5V	V_{10} min.	−5V
V_2	0 to +12V (note 2)	V_{12}	−5 to +6V
V_4	0 to +6V	V_{13}	−3 to +6.5V (note 2)
V_6	0 to +3V	V_{14}min.	−5V
V_8	−5 to +5V	V_{15}	0 to +5V

Currents (positive when flowing into the integrated circuit)

I_1	0 to +1mA	I_9	−10 to 0mA
I_3	−1 to +3mA	I_{10}max.	+3mA
I_5	−5 to 0mA	I_{14}max.	+1mA
I_6	−1 to +1mA	I_{15}	0 to +1mA
I_7	−3 to +2mA		
P_{tot}max.	Total power dissipation T_{amb} = 60°C (note 1)		580mW

Temperature

Storage temperature	−55°C to +125°C
Operating ambient temperature	−10°C to +60°C

Notes

1. Permissible during receiver switch on transient V_{11}max. 16V, P_{tot}max. 700mW for t ⩾ 60sec.
2. V_2 and V_{13} must always be lower than V_{11}

QUICK REFERENCE DATA

- Supply Voltage (Nom.) (V_{11-16}) 12V
- Supply Current (Nom.) (I_{11}) 30mA
- Luminance Signal Input Current (Typ.) ($I_{3(p-p)}$) 0.4mA
- Luminance Output Signal at Nominal Contrast Setting (Typ.) and Input Current as Above ($V_{5-16(p-p)}$) 1V (See Note 1)
- Chrominance Input Signal (Min.) ($V_{1-15(p-p)}$) 4mV
- Chrominance Input Signal (Max.) $V_{1-15(p-p)}$) 80mV
- Chrominance Output Signal at Nominal Contrast and Saturation Setting (Typ.) ($V_{9-16(p-p)}$) 1V (See Note 1)
- Contrast Control Range ⩾20dB
- Saturation Control Range ⩾20dB
- Burst Output (Closed ACC Loop) (Typ.) ($V_{7-16(p-p)}$) 1V

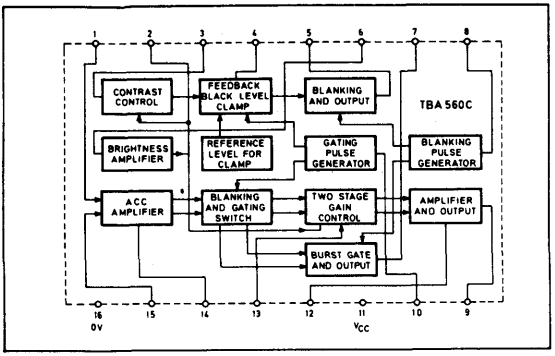


Fig. 2 TBA560C block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

V_{CC} = +12V, T_{amb} = +25°C test circuit = Fig. 6, voltages referred to pin 16

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage, V_{CC}	11	10.8	12	13.2	V	
Required Input Signals						
Chrominance input signal, p-p value of colour bars with 75% saturation, V_{1-15}	1,15	4		80	mV p-p	
Luminance input current, black-to-white	3		0.4	1.5	mA p-p	
Contrast control voltage range for 20dB control	2	2	3.7	5.6	V	See note 1 and Fig. 3
Brightness control voltage for black level of 1.5V at O/P	6		1.3		V	See note 2 and Fig. 4
Saturation control voltage range 20dB control	13	2.7	4.4	6.2	V	See note 1 and Fig. 5
Flyback blanking pulse amplitude	8					
for 0V blanking level at pin 5		0	−0.5	−1	V pk	
for 1.5V blanking level at pin 5		−2	−2.5	−3	V pk	
Burst keying (back porch) pulse (+ve going)	10	0.05		3	mA pk	
Colour killer	13	0.5		1	V	
Automatic chrominance control starting level (−ve going)	14		1.2		V	See note 3
Obtainable Output Signals						
Luminance output voltage (black-to-white)	5		1	3	V p-p	I_3 = 0.4mA p-p, V_2 = 3.7V
Black level shift				100	mV	See notes 1 and 4
Burst signal amplitude	7		1		V p-p	
Chrominance signal at nominal contrast and saturation	9		1		V p-p	See note 1
3dB bandwidth of chrominance and luminance amplifier			5		MHz	
Change of ratio of luminance to chrominance				2	dB	Contrast control 10dB

NOTES

1. Nominal contrast or saturation = maximum value −6dB. Thus, the control is +6 to −14dB on the nominal.
2. When V_6 is increased to above 1.7V, the black level of the output signal remains at 2.7V.
3. A negative-going potential provides a 26dB ACC range with negligible signal distortion. Maximum gain reduction is obtained at an input voltage of 500mV min.
4. Black level shift is specified as that due to changes of contrast and video content at constant brightness setting.

FUNCTIONAL DESCRIPTION

1. Balanced Chroma Signal Input (in conjunction with pin 15)

This is derived from the chroma signal bandpass filter, designed to provide a push-pull input. An input signal amplitude of at least 4mV peak-to-peak is required between pins 1 and 15. Both pins require DC potential of approximately +3.0V. This is derived as a common mode signal from a network connected to pin 7 (burst output). In this way DC feedback is provided over the burst channel to stabilise its operation. All figures for the chrominance signal are based on a colour bar signal with 75% saturation; i.e., burst-to-chroma ratio of input signal is 1:2.

2. DC Contrast Control

With +3.7V on this pin, the gain in the luminance channel is such that a 0.4mA black-to-white input signal to pin 3 gives a luminance output signal amplitude on pin 5 of 1V black-to-white. A variation of voltage on pin 2 between +5.6V and +2V gives a corresponding gain variation of +6 to >−14dB. A similar variation in gain in the chroma channel occurs in order to provide the correct tracking between the two signals. Beam current limiting can be applied via the contrast control network as shown in the peripheral circuit, when a separate overwind is available on the line output transformer.

3. Luminance Signal Input

This terminal has a very low input impedance and acts as a current sink. The luminance signal from the delay line is fed via a series terminating resistor and a DC blocking capacitor and requires to be about 0.4mA peak-to-peak amplitude. A DC bias current is required via a 12kΩ resistor to the +12V line.

4. Charge Storage Capacitor for Black Level Clamp

5. Luminance Signal Output

An emitter follower provides a low impedance output signal of 1V black-to-white amplitude at nominal contrast setting having a nominal black level in the range 0 to +2.7V. An external emitter load resistor is required, not less than 1kΩ. If a greater luminance output is required than 1V, with normal control settings, the input current swing at pin 3 should be increased in proportion.

6. Brightness Control

Over the range of potential +0.9 to +1.7V the black level of the luminance output signal (pin 5) is increased from 0 to +2.7V. The output signal black level remains at +2.7V when the potential on pin 6 is increased above +1.7V.

7. Burst Output

A 1V peak-to-peak burst (controlled by the ACC system) is produced here. Also, to achieve good DC stability by negative feedback in the burst channel the DC potential at this pin is fed back to pins 1 and 15 via the chroma input transformer.

8. Flyback Blanking Input Waveform

Negative going horizontal and vertical blanking pulses may be applied here. If rectangular blanking pulses of not greater than −1V negative excursion, or DC coupled pulses of similar amplitude whose negative excursion is at zero volts DC are applied, the signal level at the luminance output (pin 5) during blanking will be 0V. However, if the blanking pulses applied to pin 8 have an amplitude of −2 to −3V the signal level at the luminance output during blanking will be +1.5V. The negative pulse amplitude should not exceed −5V.

9. Chroma Signal Output

With a 1V peak-to-peak burst output signal (pin 7) and at nominal contrast and saturation setting (pins 2 and 13) the chroma signal output amplitude is 1V peak-to-peak. An external network is required which provides DC negative feedback in the chroma channel via pin 12.

10. Burst Gating and Clamping Pulse Input

A positive pulse of not less than 50μA is required on this pin to provide gating in the burst channel and luminance channel black-level clamp circuit. The timing and width of this current pulse should be such that no appreciable encroachment occurs into the sync. pulse or picture line periods during normal operations of the receiver.

11. +12V Supply (V_{CC})

Correct operation occurs within the range 10.8 to 13.2V. All signal and control levels have a linear dependency on supply voltage but, in any given receiver design this range may be restricted due to considerations of tracking between the power supply variations and picture contrast and chroma levels. The power dissipation must not exceed 580mW at 60°C ambient temperature.

12. DC Feedback for Chroma Channel (see pin 9)

13. Chroma Saturation Control

A control range of +6dB to>−14dB is provided over a range of DC potential on pin 13 from 6.2 to 2.7V. Colour killing is also achieved at this terminal by reducing the DC potential to less than +1V, e.g., from the TBA540 colour killer output terminal. The minimum "kill factor" is 40dB.

14. ACC Input

A negative-going potential gives an ACC range of about 26dB starting at +1.2V. From 1V to 800mV the steepest part of the characteristic occurs, but a small amount of gain reduction also occurs from 800mV to 500mV. The input resistance is at least 50kΩ.

15. Chroma Signal Input (see pin 1)

16. Negative Supply, 0V (Earth)

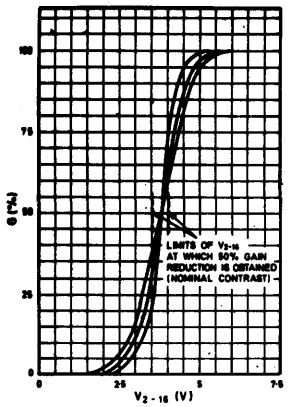


Fig. 3 Contrast control characteristic (luminance amplifier)

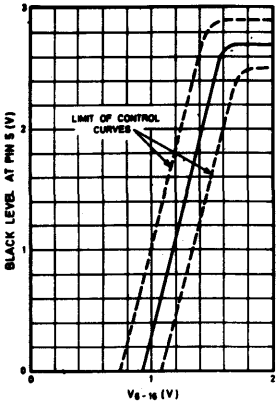


Fig. 4 Control of black level at output of luminance amplifier

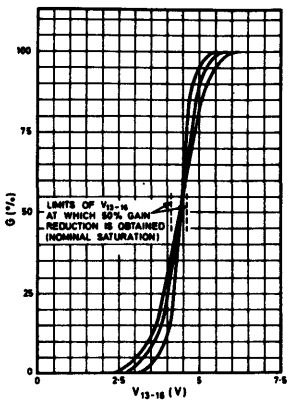


Fig. 5 Chrominance amplifier saturation characteristic

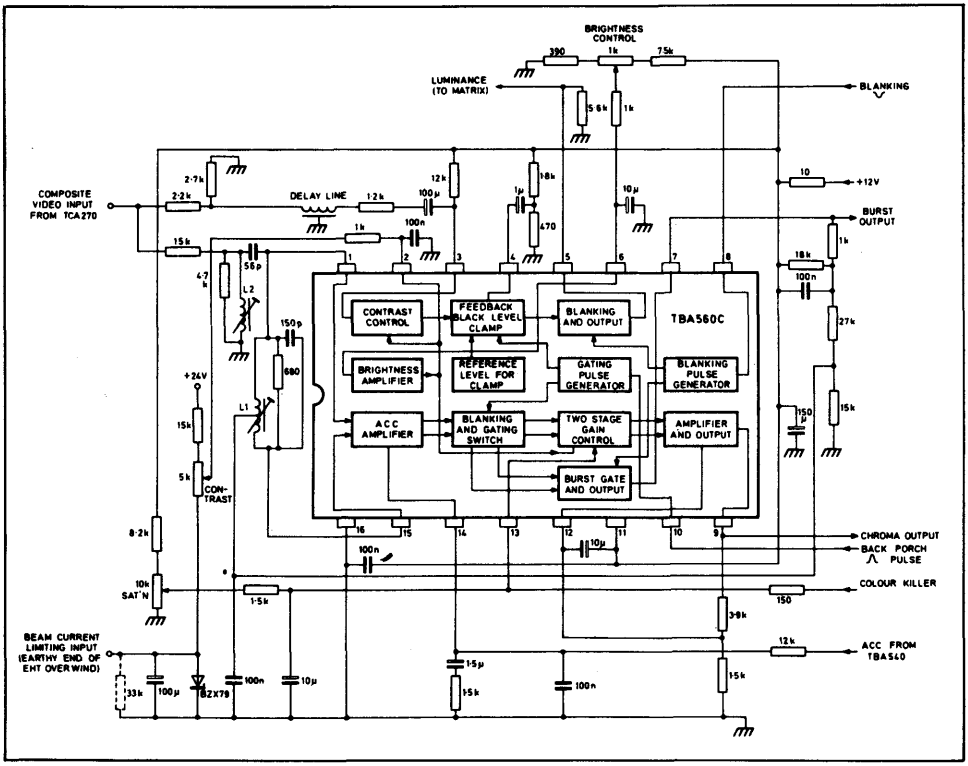


Fig. 6 Application diagram

PLESSEY
Semiconductors

TBA750B
LIMITING IF AMPLIFIER/FM DETECTOR

The TBA750B is a five-stage limiting amplifier with a balanced product detector, DC volume control, and audio driver. The circuit is suitable for all FM applications up to an intermediate frequency of 60MHz.

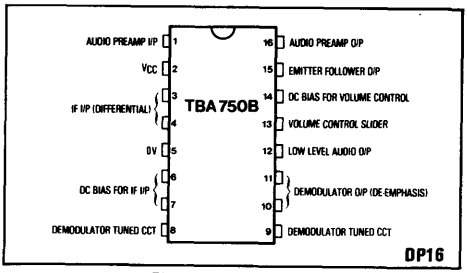


Fig.1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Supply Voltage at pin 2: +18V Power dissipation 550mW
Operating Temperature: -10°C to +65°C
Storage Temperature: -55°C to +125°C

FEATURES

- AM Rejection: 45dB at 200μV, increasing to 50dB at 2mV
- Threshold Limiting: 100μV at 6MHz
- Volume Control Range: >80dB
- Total Harmonic Distortion: 0.5% at 15kHz Deviation
- Capable of Driving a Single Transistor o/p Stage at 3W
- Audio o/p: 1.4V r.m.s. at 15kHz Deviation
- Upper 3dB point: 30MHz (Limiting Amplifier)
- Second Source Availability

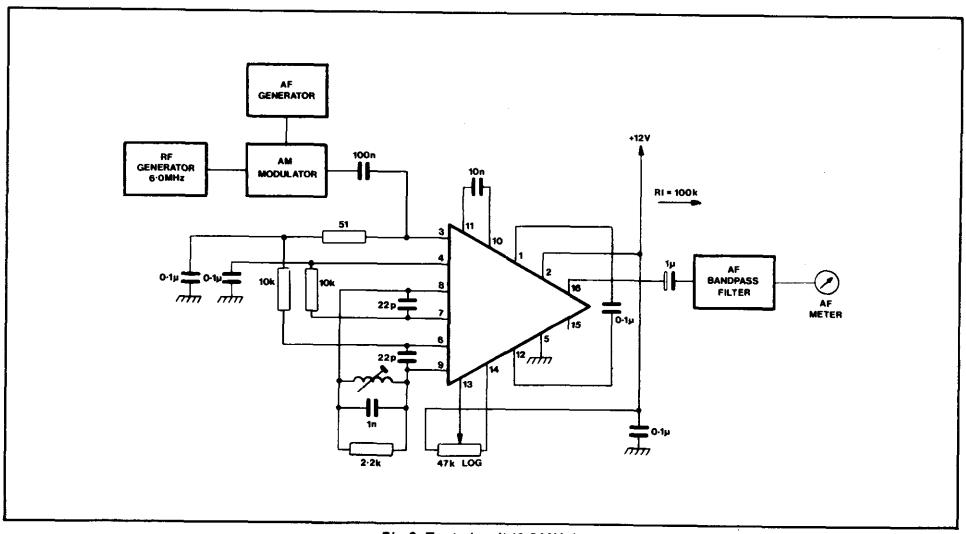
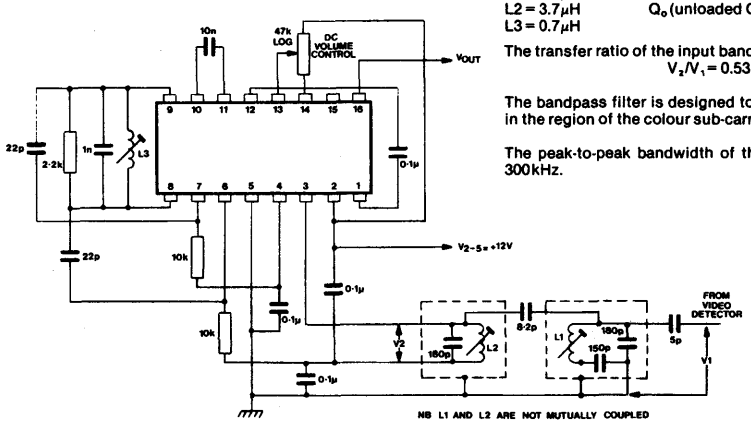


Fig.2 Test circuit (6.0MHz)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$, $V_{DD} = +12V$

Characteristics	Min.	Typ.	Max.	Units
Supply voltage range	9		12.5	V
Total current drain (at $V_{supply} = 12V$, $R_S = 0$)		23		mA
Sensitivity		100		μV
Volume Control attenuation		80		dB
A.F. Preamp gain		>8dB		dB
Input resistance	20	60		kΩ
A.M. rejection (measured in test circuit)				
$V_{in} = 0.2mV$		45		dB
$V_{in} = 1mV$		55		dB
$V_{in} = 10mV$		60		dB
$V_{in} = 100mV$		60		dB



L1 = 8.5μH
L2 = 3.7μH
L3 = 0.7μH
Q_o (unloaded Q) = 80

The transfer ratio of the input bandpass filter:
$V_2/V_1 = 0.53$

The bandpass filter is designed to give high attenuation in the region of the colour sub-carrier frequency.

The peak-to-peak bandwidth of the detector S curve is 300kHz.

Fig.3 6MHz application

PLESSEY
Semiconductors

TBA 920 TBA 920S

LINE OSCILLATOR COMBINATION

The TBA920 is a silicon integrated circuit designed for TV receiver applications. It accepts the composite video signal, separates sync. pulses with the added safeguard of noise gating and provides a sync. output for the vertical integrator. Also incorporated is the line oscillator together with two phase comparators: one to compare flyback pulses to the oscillator and the other for sync. phase comparison. The TBA920S is a special selection of the TBA920 (see Electrical Characteristics).

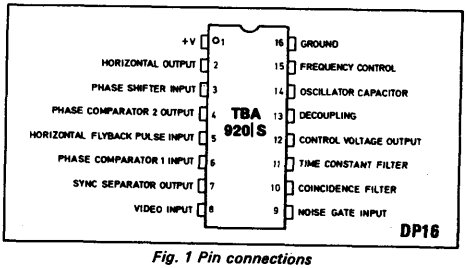


Fig. 1 Pin connections

FEATURES

- Sync separator
- Noise Gate
- Line Oscillator
- Dual Phase Comparator
- Suitable for Thyristor or Transistor Systems

QUICK REFERENCE DATA

Supply Voltage (nom.)	12V
Supply Current (nom.)	36mA
Video I/P (+ve Sync.)	3V
Flywheel Pull-in Range	±1kHz
Output Current	20mA

ABSOLUTE MAXIMUM RATINGS

Reference point is pin 16 unless otherwise stated

Supply voltage, V_{CC}	13.2V
Voltage at pin 3, V_3	0 to 13.2V
Voltage at pin 8, $-V_8$	12V
Voltage at pin 10, V_{10}	−0.5 to +5V
Average current pin 2, I_{2av}	20mA
Peak current, pin 2, I_{2pk}	200mA
Peak current, pin 5, I_{5pk}	10mA
Peak current, pin 7, I_{7pk}	10mA
Peak current, pin 8, I_{8pk}	10mA
Peak current, pin 9, I_{9pk}	10mA
Total power dissipation, P_{tot}	600mW
Storage temperature, T_{stg}	−55 to +125°C
Operating ambient temperature, T_{amb}	−10 to +60°C

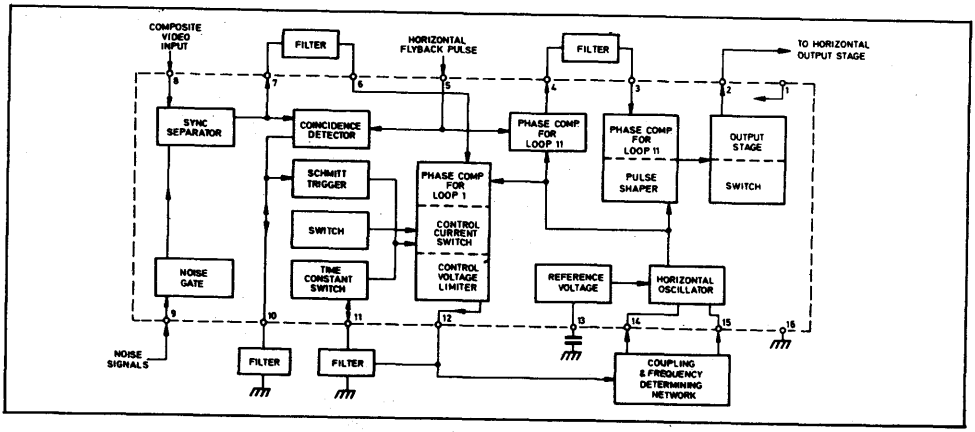


Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
V_{CC} = +12V
T_{amb} = +25°C
Reference point pin 16
Measured in test circuit Fig. 3 (CCIR standard)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Current consumption	I_1		35		mA	I_2 = 0
REQUIRED INPUT SIGNALS						
Video Signal (Pin 8)						
Input voltage, peak-to-peak	$V_{in\ p\text{-}p}$	1	3	7	V	Positive-going sync.
Peak input current during sync. pulse	I_{8pk}		100		μA	
Noise Gating (Pin 9)						
Input voltage, peak	V_{9pk}	0.7			V	
Input current, peak	I_{9pk}	0.03		10	mA	
Input resistance	R_9		200		Ω	
Flyback Pulse (Pin 5)						
Input voltage, peak	V_{5pk}		±1		V	
Input current, peak	I_{5pk}	0.05	1		mA	
Input resistance	R_5		400		Ω	
Pulse duration	t_5	10			μs	f_o = 15625 Hz
DELIVERED OUTPUT SIGNALS						
Composite Sync. Pulses, +ve, Pin 7						
Output voltage, p-p	$V_{7p\text{-}p}$		10		V	
Output resistance						
at leading edge of pulse (emitter follower)	R_7		50		Ω	
at trailing edge	R_7		2.2		kΩ	
Additional external load resistance	R_{7ext}	2.0			kΩ	
Driver Pulse (Pin 2)						
Output voltage, p-p	$V_{2p\text{-}p}$		10		V	
Average output current	I_{2av}			20	mA	
Peak output current	I_{2pk}			200	mA	
Output resistance (low ohmic)	R_2		15		Ω	
Output pulse duration when synchronised	t_2		2.5 12 to 32		Ω μs	V_2 = +10.5V, external resistor pins 2 – 16 See operating notes (1)
Permissible delay between leading edge of output pulse and flyback pulse	t_{otot}		0 to 15		μs	t_5 = 12μs
Supply voltage at which output pulses are obtained	V_{CC}	4			V	
Oscillator						
Free-running frequency	f_o		15625		Hz	R_{15} = 3.3kΩ, See operating notes (2)
Spread of frequency at nominal values of peripheral components	$\frac{\Delta f_o}{f_o}$					
TBA920				±5	%	See note 1 " "
TBA920S				±1.5	%	See note 1 " "
Frequency change when decreasing supply down to minimum 4V	$\left\|\frac{\Delta f_o}{f_o}\right\|$			10	%	
Frequency control sensitivity	$\frac{\Delta f_o}{\Delta I_{15}}$		16.5		Hz/μA	
Adjustment range of network in circuit of Fig. 3	$\frac{\Delta f_o}{f_o}$		±10		%	

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Influence of supply voltage on frequence at V_p = 12V	$\frac{\delta f_0/f_0}{\delta V_p/V_{pnom}}$			5	%	
Control Loop I (Between Sync. Pulse and Oscillator)						
Control voltage range	V_{12}		0.5 to 5.5		V	
Control current, peak	I_{2pk}		±2		mA	V_{10}>4.5V, V_6>1.5V
			±6		mA	V_{10}<2V, V_6>1.5V
Loop gain of APC system	$\frac{\Delta f}{\Delta t}$		1		kHz/μs	Time coincidence between sync. pulse and flyback pulse or V_{10}>4.5V
			3		kHz/μs	No time coincidence or V_{10}<2V
Capture and holding range	Δf		±1		kHz	See note 2
Pull-in time	t		20		ms	$\Delta f/f_0$ = ±3% (Δf≈470Hz), see Fig. 3
Switch-over from high control sensitivity to low control sensitivity after capture	t		20		ms	See Fig. 3
Control Loop II (Between Flyback Pulse and Oscillator)						
Permissible delay between leading edge of output pulse (pin 2) and leading edge of flyback pulse	t_{dtot}		0 to 15		μs	
Static control error	$\frac{\Delta t}{\Delta t_d}$			0.5	%	See operating notes (3)
Peak output current during flyback pulse	I_{4pk}		±0.7		mA	
Overall Phase Relation						
Phase relation between leading edge of sync. and middle of flyback pulse	t		4.9		μs	See operating notes (4)
Tolerance of phase relation	Δt					
TBA920				±0.7	μs	See operating notes (5)
TBA920S				±0.4	μs	See operating notes (5)
Voltage for t_2 = 12 to 32μs	V_3		6 to 8		V	
Adjustment sensitivity	$\frac{\Delta t_2}{\Delta V_3}$		10		μs/V	
Input current	I_3			2	μA	
External Switch-over of Parameters (Loop Filter and Loop Gain) of Control Loop I (e.g. for Video Recorder Application). See Note 3						
Required switch-over voltage	V_{10}	4.5			V	R_{11} = 150Ω
				2.0	V	R_{11} = 2kΩ
Required switch-over current	I_{10}		80		μA	R_{11} = 150Ω, V_{10} = 4.5V
			120		μA	R_{11} = 2kΩ, V_{10} = 2.0V

NOTES
1. Exclusive of external component tolerances
2. Adjustable with R_{12-15}
3. With sync. pulses at pins 7 and 8, without RC network at pin 10

OPERATING NOTES

1. The output pulse duration is adjusted by shifting the leading edge (V_3 from 6V to 8V). The pulse duration is a result of delay in the line output device and the action of the second control loop in the TBA920.
For a line output stage with a BU108 high voltage transistor the resulting duration is about 22μs, and in such a way that the line output transistor is switched on again about 8μs after the middle of the line flyback pulse. This pulse duration must be taken into account when designing the driver stage and driver transformer as this way of driving the line output device differs from the usual, i.e. a driver duty cycle of about 50%.
2. The oscillator frequency can be changed for other TV standards by an appropriate value of C_{14}.
3. The control error is the remaining error in reference to the nominal phase position between leading edge of the sync. pulse and the middle of the flyback pulse caused by a variation in delay of the line output stage.
4. This phase relation assumes a luminance delay line with a delay of 500ns between the input of the sync. separator and the drive to the picture tube. If the sync. separator is inserted after the luminance delay line or if there is no delay line at all (monochrome sets), then the phase relation is achieved at $C^{5}/_{16}$ = 560pF.
5. The adjustment of the overall phase relation and consequently the leading edge of the output pulse at pin 2 occurs automatically by the control loop II or by applying a DC voltage to pin 3.

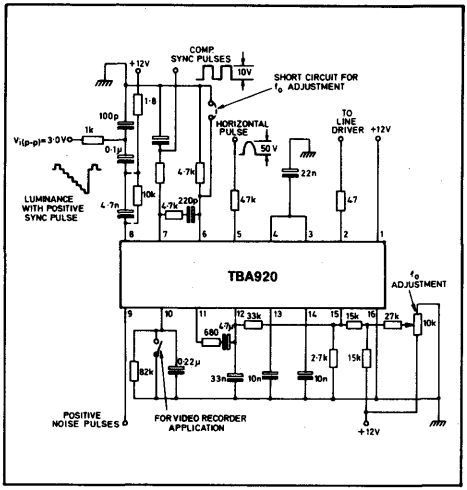


Fig. 3 Application diagram

PLESSEY
Semiconductors

TBA950 : 2X

LINE OSCILLATOR COMBINATION

The TBA950:2X is a monolithic integrated circuit for pulse separation and line synchronisation in TV receivers with transistor output stages.

The TBA950:2X comprises the sync. separator with noise suppression, the frame pulse integrator, the phase comparator, a switching stage for automatic changeover of noise immunity, the line oscillator with frequency range limiter, a phase control circuit and the output stage.

It delivers prepared frame sync. pulses for triggering the frame oscillator. The phase comparator may be switched for video recording operation. Due to the large scale of integration few external components are needed.

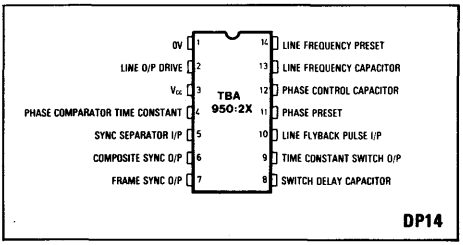


Fig. 1 Pin Connections

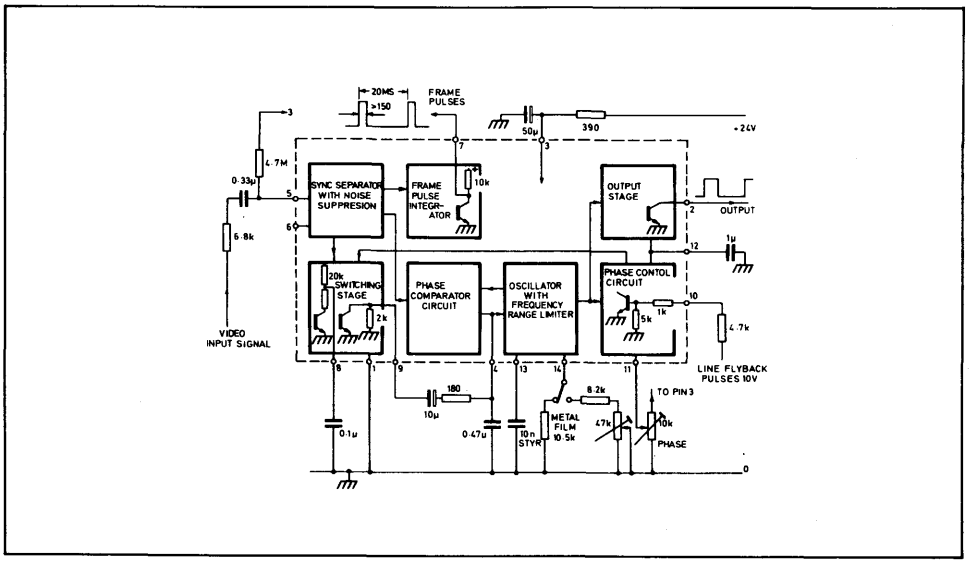


Fig. 2 Block diagram and test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$
$f_o = 15625Hz$ in the test circuit Fig.2 (see note 1)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Amplitude of frame pulse	V_1		>8		V	
Frame pulse duration	t_7		>150		µs	
Output resistance at pin 7 (high state)	$R_{out\ 7}$	7.5	10	13	kΩ	
Amplitude of sync. pulse	V_6		>8		V	
Output resistance at pin 6	$R_{out\ 6}$	2.5		4.5	kΩ	
Output pulse duration	t_2	25		28.5	µs	Typical range
Residual output voltage	$V_{2\ res}$		<0.55		V	$I_2 = 20mA$
Oscillator frequency	f_o	14843	15625	16406	Hz	$C_{13/1} = 10nF$ $R_{14/1} = 10.5k\Omega$
Frequency pull-in range	$\pm\Delta f_F$	400		1000	Hz	Typical range
Frequency holding range	$\pm\Delta f_H$	400		1000	Hz	Typical range
Slope of phase comparator control loop	df_o/dt_d		2		kHz/µs	
Gain of phase control	dt_d/dt_p		20			
Phase shift between leading edge of composite video signal and line flyback pulse (see note 2) adjustable by V_{11}	t_v	−1		3.5	µs	Typical range

NOTES
1. By modification of the frequency-determining network at pins 13 and 14, these ICs can also be used for other line frequencies.
2. The limited flyback pulse should overlap the video signal sync. pulse on both edges.

OPERATING NOTES

The sync. separator separates the synchronizing pulses from the composite video signal. The noise inverter circuit, which needs no external components, in connection with an integrating and differentiating network frees the synchronizing signal from distortion and noise.

The frame sync. pulse is obtained by multiple integration and limitation of the synchronizing signal, and is available at pin 7. The *RC* network hitherto required between sync. separator and frame oscillator is no longer needed. Since the frame sync. pulse duration at pin 7 is subject to production spreads it is recommended to use the leading edge of this pulse for triggering.

The frequency of the line oscillator is determined by a 10 nF polystyrene capacitor at pin 13 which is charged and discharged periodically by two internal current sources: The external resistor at pin 14 defines the charging current and consequently in conjunction with the oscillator capacitor the line frequency.

The phase comparator compares the sawtooth voltage of the oscillator with the line sync. pulses. Simultaneously an AFC voltage is generated which influences the oscillator frequency. A frequency range limiter restricts the frequency holding range.

The oscillator sawtooth voltage, which is in a fixed ratio to the line sync. pulses, is compared with the flyback pulse in the phase control circuit, in this way compensating all drift of delay times in driver and line output stage. The correct phase position and hence the horizontal position of the picture can be adjusted by the 10 kΩ potentiometer connected to pin 11. Within the adjustable range the output pulse duration (pin 2) is constant. Any larger displacements of the picture, e.g. due to non-symmetrical picture tube, should not be corrected by the phase potentiometer, since in all cases the flyback pulse must overlap the sync. pulse on both edges (see Fig. 3).

The switching stage has an auxiliary function. When the two signals supplied by the sync. separator and the phase control circuit respectively are in synchronism a saturated transistor is in parallel with the integrated 2 kΩ resistor at pin. 9. Thus the time constant of the filter

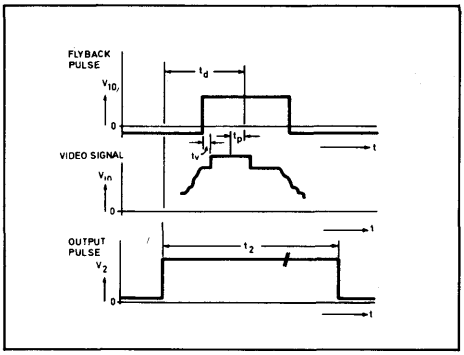


Fig. 3 Phase relationships

network at pin 4 increases and consequently reduces the pull-in range of the phase comparator circuit for the synchronized state to approximately 50Hz. This arrangement ensures disturbance-free operation.

For video recording operation this automatic switch-over can be blocked by a positive current fed into pin 8, e.g. via a resistor connected to pin 3. It may also be useful to connect a rsistor of about 630 Ω or 1 kΩ between pin 9 and earth. The capacitor at pin 4 may be lowered, e.g. to 0.1µF. These alterations do not significantly influence the normal operation of the IC and thus do not need to be switched.

The output stage delivers at pin 2 output pulses of duration and polarity suitable for driving the line driver stage. If the supply voltage goes down (e.g. by switching off the mains) a built-in protection circuit ensures defined line frequency pulses down to $V_3 = 4V$ and shuts off when V_3 falls below 4V, thus preventing pulses of undefined duration and frequency. Conversely, if the supply voltage rises, pulses defined in duration and frequency will appear at the output pin as soon as V_3 reaches 4.5V, In the range between $V_3 = 4.5V$ and full supply the shape and frequency of the output pulses are practically constant.

RECOMMENDED OPERATING CONDITIONS

For operating circuits Figs. 4 and 5

Input current during sync. pulse I_5 $>5\mu A$
Composite video input signal $V_{in\ p\text{-}p}$ 3(1 to 6)V
Input current during line flyback pulse I_{10} 0.2 to 2 mA
Switchover current I_8 $>2mA$
Time difference between the output pulse at pin 2 and the line flyback pulse at 10, t_d $<20\mu s$
Current consumption (see Fig. 6) I_3 $<31mA$
Ambient operating temperature range, T_{amb} 0 to +60°

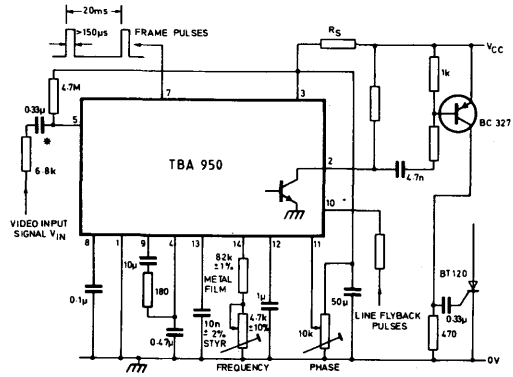


*Fig. 4 Operating circuit (thryistor output stage) *Input circuitry must be optimised*

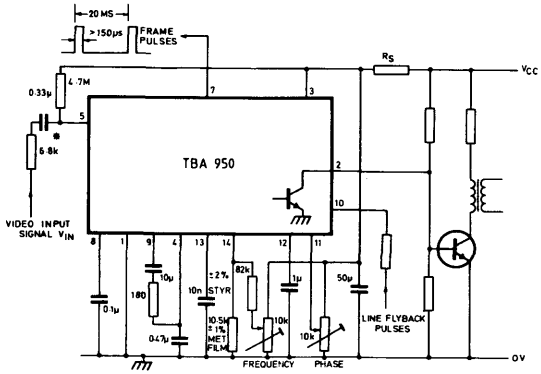


*Fig. 5 Another possiblity for line frequency adjustment (transistor output stage) *Input circuitry must be optimised*

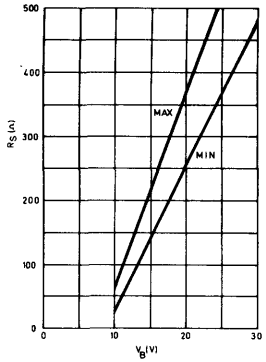


Fig. 6 Graph for determining the supply series resistor R_5

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to pin 1

Supply current (see Fig. 6) I_5:	45mA
Input current I_5:	2mA
Input voltage V_5	−6V
Output current I_2	22mA
Output voltage V_2:	12V
Switch-over current for video recording I_8	5mA
Phase correction voltage V_{11}:	0 to V_3
Operating temperature range	−10°C to +60°C
Storage temperature range	−55°C to +125°C

PLESSEY
Semiconductors

TCA800

COLOUR DEMODULATOR WITH FEEDBACK CLAMPS

A monolithic integrated circuit for colour television receivers incorporating two active synchronous demodulators for the F_{B-Y} and $\pm F_{R-Y}$ signals, a G-Y matrix, PAL switch bistable and RGB matrix, suitable for driving simple single transistor video output stages. The circuit incorporates three feedback clamps to stabilise the black level, to eliminate the problem of thermal drift in the demodulators.

OPERATING NOTES

For alternative applications in a simple decoder circuit, it must be possible to trigger the flip-flop so that it runs in the correct ident. phase by means of an AC coupled, 2 volt p-p square wave, derived from the APC loop in the reference generator circuit. (The normal input line timebase pulse would still be applied in order to provide clamp pulses.)

Input impedance of output amplifier (BF337) (Expressed as parallel resistance and capacitance.)

R (typ.) 5kΩ
C (typ.) 80pF

The above values are given for suitable design of output stages i.e. emitter follower with 5mA current capability.

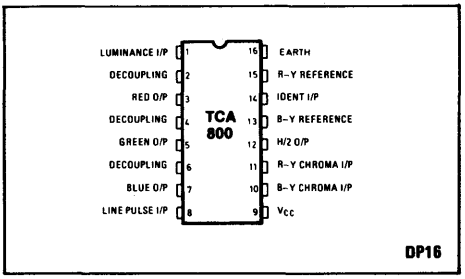


Fig. 1 Pin connections

QUICK REFERENCE DATA

V_{supply} -(Nominal) 12V
I_{supply} -(Nominal) (I_B = 0.5mA) 47mA
Voltage Gain of Chrominance (R-Y) Signal Channel (typ.) $V_{in(p-p)}$ = 50mV; f = 4.43MHz; Video Gain = X20 17.5V/V
Voltage Gain of Luminance (Y) Channel V_{in} (Black-to-White) = 1V (p-p) 5V/V
Operating Temperature Range −10 to +55°C

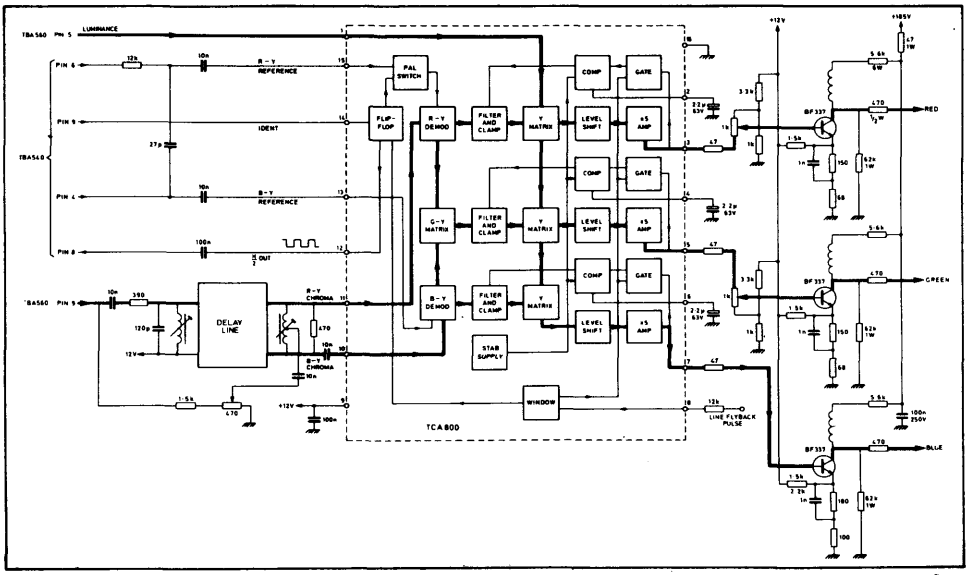


Fig. 2 Block diagram and typical application circuit

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

T_{amb} = +25°C, V_{CC} = +12V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage range	9	10.8	12	13.2	V	
Voltage gain of chrominance (R-Y) signal channel			17.5		V/V	$V_{in\ p\text{-}p}$ = 50mV, f = 4.43MHz, video gain = X20
Voltage gain of luminance (Y) channels			5		V/V	$V_{in\ (black\text{-}to\text{-}white)}$ = 1V p-p
Bandwidth (−3dB) of luminance channel from Y input to R-G-B outputs			10		MHz	
Bandwidth (−3dB) of chroma channel from $F_{(R-Y)}$, $F_{(B-Y)}$ inputs to R-G-B outputs			1		MHz	
Ratio of demodulated signals						
$V_{(B-Y)}/V_{(R-Y)}$		1.60	1.78	1.96		Defined with equal chroma input signals
$V_{(G-Y)}/V_{(R-Y)}$		0.76	0.85	0.94		and measured at output pins (see note 1)
Input Characteristics						
Chrominance input impedance (expressed as resistance and parallel capacitance	10, 11					
R			1000		Ω	f = 4.43MHz, V_{in} = 20mV sinewave
C				10	pF	
Luminance (Y) input blanking level (fixed by TBA560)	1	1.4	1.5	1.8	V	
Luminance (Y) input, black level potential (nominal brightness set by brightness control of TBA560)	1		1.7		V	
Luminance (Y) input black-to-white amplitude (adjusted by contrast control of TBA560)	1		1.0		Vp-p	
Reference input impedance (expressed as resistance and parallel capacitance)	13, 15					
R			5.0		kΩ	f = 4.43MHz
C			5.0	10	pF	
Reference input voltage (from TBA540)	13, 15	0.5	1.0	2.0	V p-p	
Phase shift between reference inputs and chroma input signal to give coincidence at the synchronous demodulators	13, 15		10		degrees	
Ident. voltage for ident 'off'	14	+6			V	
Ident. voltage for ident 'on'	14			+7.0	V	
Ident. current for ident 'off'	14			0.1	mA	
Tracking of ident. threshold with a supply variation of ±10%						
$\frac{\Delta V_{threshold} \cdot V_{CC}}{V_{threshold} \cdot \Delta V_{CC}}$	14		1.0			
Required line pulse input current to clamps and H/2 flip-flop	8	0.3	0.45	0.6	mA	
Window level (see note 2)	8		+12.5		V	
Line input impedance	8	0.6	1.0	1.4	kΩ	
Output Characteristics						
R-G-B outputs blanking level	3, 5, 7		2.0		V DC	Blanking level at pin 1 = 1.5V
Common mode variation of black level variation over a temperature range of 40°C		See note 3				
Blanking-to-white level output voltage capability of each output amplifier channel	3, 5, 7	6		8	V p-p	

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Difference in clamped blanking level of outputs i.e., R to G to B	3,5,7			50	mV	
Differential drift of clamped output blanking levels over temperature range of 40°C	3, 5, 7			25	mV	
Residual 4.43MHz signal at R-G-B outputs						
Red				150	mV p-p	
Blue				300	mV p-p	
H/2 square wave output amplitude	12	2.5	3.5		V p-p	Measured with 3kΩ load i.e. TBA540

NOTES

1. These values are chosen to minimise errors in flesh tones and of the luminance of the green component. The matrix equation for the derivation of the G-Y component is given by G-Y = −0.51(R-Y) −0.19(B-Y). (This is derived from the basic colour equation Y = 0.30R + 0.59G +0.11B.) Measured at the tube cathodes with 100V p-p video drive.
2. In order to provide a clamp pulse which occurs inside the blanking waveform and free from the edge spikes, it is necessary to window the line pulse at about two thirds of its amplitude.
3. In order to partially compensate for drift in output stages a negative temperature coefficient to compensate for the variation in the video output transistor has been incorporated.

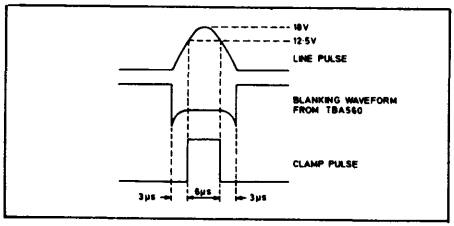


Fig. 3 Line pulse, blanking and clamp timings

ABSOLUTE MAXIMUM RATING

Max. dissipation @ +55°C = 900mW
Storage temperature range −55°C to +125°C

PLESSEY
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TDA 440

VIDEO IF AMPLIFIER/DEMODULATOR

The TDA440 incorporates the following functions:

1. Three-stage symmetrical IF (broad band) amplifier with first and second stages AGC-controlled.
2. Controlled video carrier demodulator.
3. Video drive amplifier with low-pass response and output independent of supply fluctuations.
4. Gated AGC section for IF amplifier.
5. Delayed regulated output voltage for the tuner preamplifier.

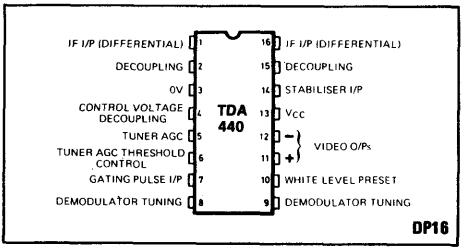


Fig. 1 Pin connections.

FEATURES

- High Gain – High Stability
- Constant Input Impedance Independent of AGC
- Low Noise Independent of AGC
- High Supply Rejection
- Low RF Breakthrough to Video O/Ps
- Fast AGC Action
- Very Low Intermodulation Products
- Minimum Differential Error
- Positive and Negative Video O/Ps
- Low Impedance Video O/Ps
- Temperature Compensated
- Peak White Adjustable

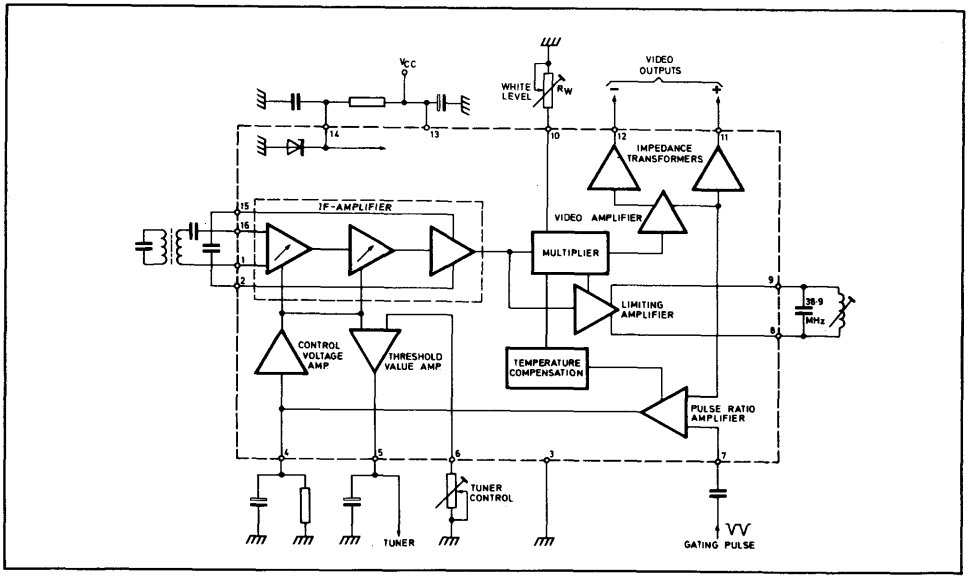


Fig. 2 TDA440 block diagram.

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

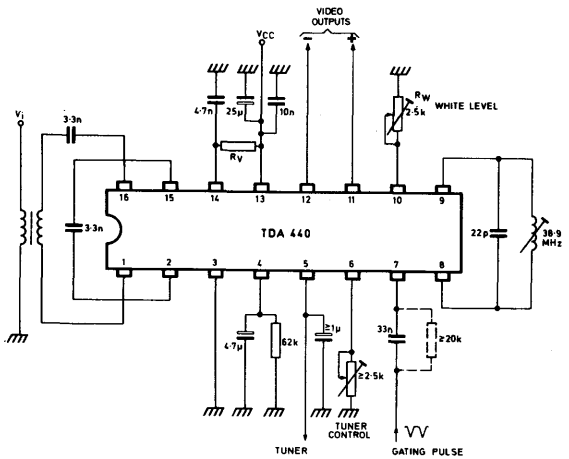
T_{amb} = +25°C
V_{CC} = +12V
Reference point is pin 3

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage, V_{CC}	13	10	12	15	V	
Supply current, I_{13}	13	15	19	25	mA	
Supply voltage, stabiliser input	14	5.5	5.8	6.4	V	I_{14} = 40mA
Positive video DC output voltage	11		5.5		V	
White level adjustment range for positive video DC output voltage	11			4.8	V	R_w (pin 10) = ∞
		6.5			V	R_w (pin 10) = 0
Peak black clamping level for positive video DC output voltage	11	1.75	1.9	2.15	V	
DC output current	11		3.2		mA	Reference point pin 13
Negative video DC output voltage	12		5.6		V	
Available tuner control current	5	7	7.5		mA	10dB after onset of tuner control action
Negative gating pulse	7	1.5	3	5	Vp-p	
Composite video output level	11		3.3		Vp-p	V_{11} = 5.5VDC
			4.2		Vp-p	V_{11} = 6.4VDC
AGC range, ΔAGC		50	56		dB	
Video 3dB bandwidth		8	10		MHz	
Video frequency response change			1.0	2.0	dB	ΔAGC = 50dB, video bandwidth = 0 to 5 MHz
Symmetrical input voltage for 3.3Vp-p output (pin 11)	1-16	100	150	220	μVr.m.s	
Maximum IF voltage level present at video outputs over the full AGC range	11,12			30	mV	f = 38.9MHz
				50	mV	f = 77.8MHz (2nd harmonic)
Sound IF voltage level present at video outputs with selective circuit	12	30			mV	f = 5.5MHz, $\frac{\text{picture carrier level}}{\text{sound carrier level}}$ = 30dB
Differential gain of negative comp. video output signal for full black to white swing				15	%	
Suppression of sound carrier/colour subcarrier (1.07MHz) w.r.t colour subcarrier level		40			dB	Picture carrier = 0dB, IF colour subcarrier level = −6dB, IF sound carrier level = −24dB
Input impedance	1					Reference point pin 16
AGC max.			1.4//2		kΩ//pF	
AGC min.			1.4//1.9		kΩ//pF	

ABSOLUTE MAXIMUM RATINGS

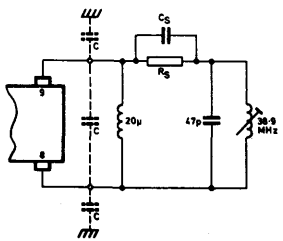
Reference point is pin 3

Rating	Pin	Symbol	Value	Units
Supply voltage range	13	V_{CC}	10 to 15	V
Low voltage stabiliser supply current	14	I_s	50	mA
Open loop voltage	5	V_5	15	V
Video DC output current				
Average positive	12	I_{12}	5	mA
Peak positive	12	I_{12}	30	mA
Average negative	11	I_{11}	5	mA
Peak negative	11	I_{11}	30	mA
White level control	10	V_{10}	3.2	V
Power dissipation at $T_{amb} \leqslant 55°C$		P_{tot}	700	mW
Ambient temperature range		T_{amb}	−10 to +65	°C
Storage temperature range		T_{stg}	−55 to +125	°C



Supply voltage *must be disconnected* before inserting the integrated circuit into the test socket.

Fig. 3 Test and application circuit.



C = Parasitic capacitance at pins 8 and 9 should be kept to a minimum.
C_S = 6 to 10pF series capacitance.
f_O = Series resonant frequency = 38.9 − (1.8 to 2.75) MHz.
R_S = Series resonance damping (determines tuning characteristics) = 1.8 to 3.3kΩ E.G., with R_S = 2.4kΩ, tuning range, f, = 3MHz.

Fig. 4 Modifications to Fig. 3 for improving audio interference and cross-colour characteristics.

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PRELIMINARY INFORMATION

Preliminary Information is issued to advise Customers of potential new products which are designated *'Experimental'* but are, nevertheless, serious development projects. Details given may, therefore, change without notice and no undertaking is given or implied as to current or future availability. Customers incorporating *'Experimental'* product into their equipment designs do so at their own risk. Please contact your local Plessey Semiconductors Sale Office for details of current status.

TDA1365

COMPLETE LUMA/CHROMA PROCESSOR

The TDA1365 is a bipolar integrated circuit for use as a complete TV colour signal processor. Designed to decode PAL signals directly, it can be extended to decode SECAM signals with automatic standards switching. All the circuitry required for both Luminance and Chrominance signal processing is included with the facility of DC control of Brightness, Contrast and Colour.

The device requires minimal external components and adjustments and is encapsulated in a 28-lead, dual in-line, plastic package (DP28).

FEATURES

- Complete Luminance and Chrominance Signal Processing in a Single Package
- Low External Component Count
- Minimal External Adjustments
- Single 12 V Supply
- Low Dissipation
- Low Cost, Single Chip Solution
- Fast Data Blanking Facility

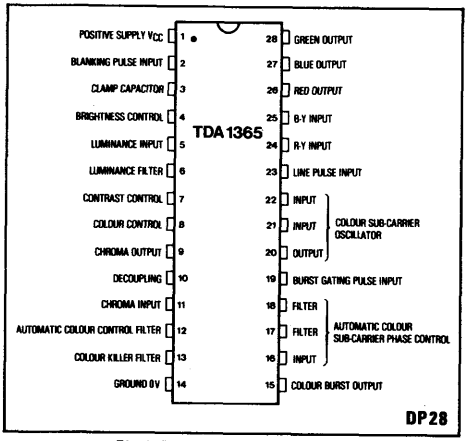

Fig.1 Pin connections (top view)

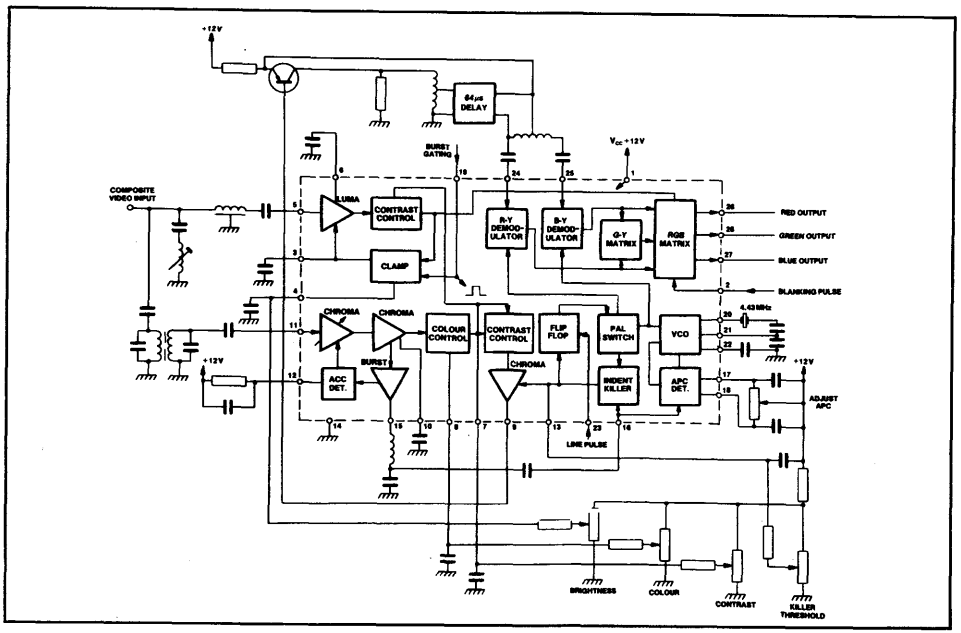

Fig.2 TDA1365 block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
V_{CC} = 12V, T_{amb} = +25°C
Luminance input pin 5: 1V_{p-p} negative video
Chrominance input pin 11: 150mV_{p-p} burst level

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	1	10.5	12	13.5		
Supply current	1	—	43	54	mA	
Burst gating pulse input	19	2	3	6	V_{p-p}	
Line pulse input	23	1.5	2	6	V_{p-p}	
Blanking pulse input	2	2	3	6	V_{p-p}	
Control voltage input	4, 7, 8, 13	3.5	—	8	V	Typical range
Demodulator input	24, 25	—	200	—	mV_{p-p}	
Subcarrier oscillator pull-in frequency range	20	±300	±500		Hz	
Differential gain of luminance channel	26, 17, 28	—	—	5	%	Input 1V_{p-p} staircase Output block level = 2V
RGB output voltage normal	26, 27, 28	—	3.5	—	V_{p-p}	
RGB output voltage maximum	26, 27, 28	7	—	—	V_{p-p}	
RGB quiescent output voltage	26, 27, 28	2.5	3.3	4.1	V	No luminance Input V4 = 9V V7 = 7V
Temperature coefficient		-2	0	+2	mV/°C	

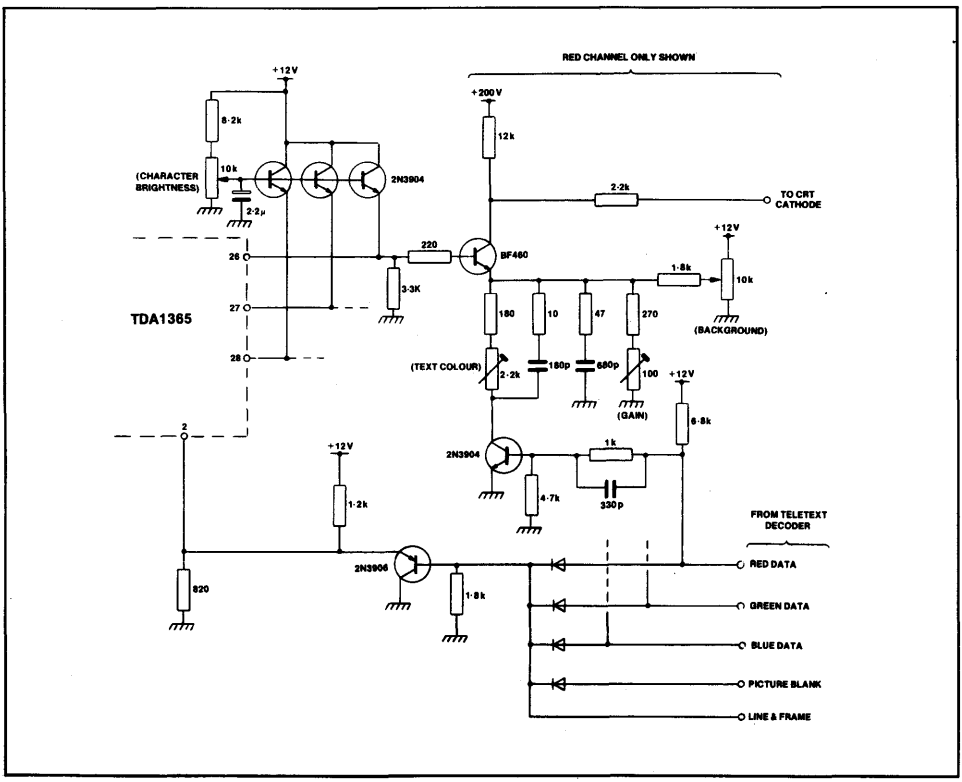

Fig.3 Typical output stage with data inputs

ABSOLUTE MAXIMUM RATINGS

Supply voltage	−0.5 V to +15 V
Input voltage pins 5 and 11	$5V_{p-p}$
Input voltage pins 2, 19 and 23	±6 V
Maximum power dissipation	750 mW
Operating temperature range	−10 °C to +65 °C
Storage temperature range	−55 °C to +125 °C

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TDA 2522/3

COLOUR DEMODULATOR COMBINATION

The TDA2522 and TDA2523 are integrated synchronous demodulators for colour television receivers. The devices incorporate an 8.8MHz oscillator followed by a divider giving two 4.4MHz reference signals, a keyed burst phase detector for optimum noise behaviour, an ACC detector and amplifier, a colour killer, two synchronous demodulators for the (B-Y) and (R-Y) signals, a PAL switch and a PAL flip-flop with internal identification.

The symmetrical demodulators include integrated capacitors to reduce unwanted carrier signals at the outputs which are taken from temperature-compensated emitter followers. The outputs of the TDA2522 are suitable for use with the TDA2530. The TDA2523 outputs are inverted for use with a direct transistor drive.

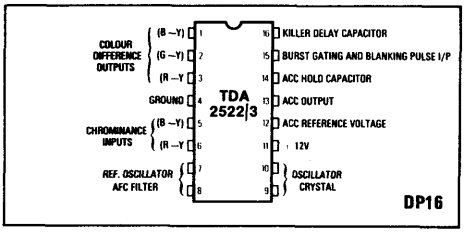

Fig. 1 Pin connections

QUICK REFERENCE DATA

- Supply Voltage (pin 11): 12V typ.
- Supply Current: 40mA typ.
- Colour Difference Signals:
  (R–Y) (pin 3): >2.4V p–p
  (G–Y) (pin 2): >1.35V p–p
  (B–Y) (pin 1): >3V p–p
- Chrominance Input Signal (Including Burst):
  R–Y (pin 6) 500mV p–p
  B–Y (pin 5) 350mV p–p
- Colour Difference Signal Output Impedance 250 Ω typ.

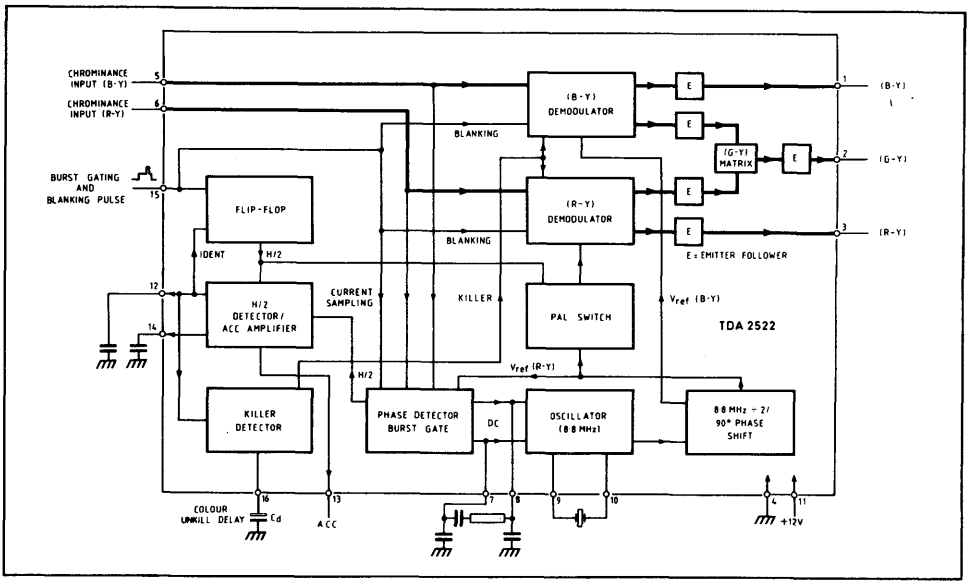

Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions unless (otherwise stated):
Supply voltage, pin 11 = +12V
Tamb = +25°C
Measurements referred to pin 4

Charateristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Demodulator						
Ratio of demodulated signals:						
B–Y/R–Y	1/3		1.78		–	
G–Y/R–Y	2/3		0.85		–	See note 1
G–Y/R–Y	2/3		0.17		–	See note 2
Colour difference outputs:						
(R–Y)	3	2.4			Vp–p	
(G–Y)	2	1.35			Vp–p	
(B–Y)	1	3			Vp–p	
Chrominance input signal (including burst):						
R–Y	6		500		mVp-p	See note 3
B–Y	5		350		mVp–p	See note 3
Colour difference signal output impedances:						
(R–Y)	3		250		Ω	
(G–Y)	2		250		Ω	
(B–Y)	1		250		Ω	
H/2 ripple at R–Y O/P	3			10	mVp-p	
Blanking and keying pulse:						
Burst keying active for	15	7.5			Vp–p	
Burst keying inactive for	15			6.5	Vp–p	
Blanking active for	15	2			Vp–p	
Blanking inactive for	15			1	Vp–p	
Reference section						
Phase difference between reference and burst				±5	Deg.	Crystal frequency deviation ±400Hz
Overall holding range			±500		Hz	Using typical crystal
Burst signal input	5–6		0.25		Vp–p	Keying pulse width = 4μs,
Oscillator input resistance	10		270		Ω	
Oscillator input capacitance	10				pF	See note 5
Oscillator output resistance	9		200		Ω	
ACC reference voltage	12		7		V	
ACC voltage at correct phase	14		5.5		V	Burst = 0.25Vp–p
ACC voltage with zero burst	14		7.0		V	Burst = 0.25Vp–p
ACC amplifier output voltage range	13	0.5		5.0	V	$I_{13} < \pm 200\mu A$
Colour killer						
Via pin 14:						
Colour off	14	6			V	
Colour on	14			5.6	V	
Via pin 16:						
Colour off	16	7			V	
Colour on	16			5	V	
Colour unkill delay			20		ms/μF	See note 6

NOTES
1. The demodulators are driven by a chrominance signal of equal amplitude for the (R—Y) and (B—Y) components. The phase of the (R—Y) chrominance signal equals the phase of the (R—Y) reference signal. The same holds for the (B—Y) signals.
2. As note 1, but with the phase of the (R—Y) reference signal reversed.
3. Colour bar with 75% saturation.
4. The burst amplitude is kept constant by ACC action, but depends linearly on the keying pulse width.
5. To be established.
6. The delay depends on the value of Cd (see Fig. 2)

FUNCTIONAL DESCRIPTION

Functions listed by pin number.

TDA2522	TDA2523
1. -(B-Y) signal output	(B-Y) signal output
2. -(G-Y) signal output	(G-Y) signal output
3. -(R-Y) signal output	(R-Y) signal output

These outputs are of low impedance from temperature compensated emitter follower stages that require external loads of 10kΩ. Internal filtering of the colour difference output signals to give a −3dB bandwidth of 1MHz allows the three signals to be fed directly to the luminance matrix. The TDA2522 may be AC coupled to the TDA2530, and the TDA2523 may be used with direct transistor drive.

4. Negative supply (Ground)

5. Chrominance B−Y input signal

An input signal of approximately 350mV p-p (colour bars) is required at this pin. The B−Y component of colour burst must be included with the input chrominance signal.

6. Chrominance R−Y input signal

An input signal of approximately 500mV p-p (colour bars) is required, including the R−Y colour burst component.

7. Reference oscillator APC loop filter

8. Reference oscillator APC loop filter

Between pins 7 and 8 are connected the APC loop low pass filter components. The difference voltage between these pins is connected internally to the oscillator reactance stage.

9. Oscillator feedback

10. Oscillator feedback

A series network consisting of the 8.8MHz crystal and an adjustable tuning capacitor is connected between pins 9 and 10. Division from the 8.8MHz oscillator within the IC produces the 4.4MHz quadrature reference carriers which are then applied to the colour demodulators.

11. Positive 12V supply

The maximum voltage must not exceed 14V.

12. ACC hold capacitor

The capacitor connected from this pin to ground is normally charged to a potential of about 7V.

13. ACC output potential

An output potential varying inversely with the input colour burst amplitude is available at pin 13. Maximum ACC gain of the TDA2560 is provided when the ACC potential from pin 13 of the device is greater than about 1.4V.

14. ACC hold capacitor

The capacitor connected from this pin to ground is normally charged to a potential of 5.5V. On monochrome reception the potential will be 7.0V and while identing it may instantaneously increase to about 8V. A 100Ω resistor may be connected in series with the capacitor from pin 14, see pin 15.

15. Burst gating and blanking pulse input.

The two-level positive pulse required at this pin is used for burst gating and flip-flop triggering, at a sampled level of 7V. A negative going pulse of about 100mV p-p, derived from the colour burst, may be inspected across a 100Ω resistor in series with the capacitor from pin 14 to ground, should the sandcastle pulse shape require some adjustment. At a level of about 1.5V the pulse width should be suitable for chroma blanking.

16. Killer delay capacitor

The value of a capacitor connected from pin 16 to ground determines the delay of un-killing. By this means the state of continuous switching of the killer with marginal signals, may be avoided. Connecting pin 16 to ground unkills the system.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (pin 1)	14V
Total power dissipation	600mW
Storage temperature	−55°C to +125°C
Operating ambient temperature	−10°C to +60°C

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TDA2530/2

RGB Matrix Preamplifier (with clamps)

The TDA2530 and TDA2532 are integrated RGB matrix preamplifiers for colour television receivers, incorporating a matrix preamplifier (for RGB cathode drive of the picture tube) with clamping circuits.

This integrated circuit has been designed to be driven from the TDA2522 synchronous demodulator and oscillator IC.

The TDA2532 has been designed for use with on-screen data display systems.

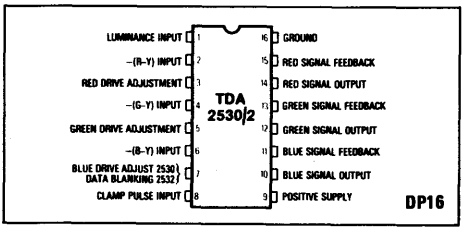

Fig. 1 Pin connections (top view)

QUICK REFERENCE DATA

- Supply Voltage (pin 9): 12V typ.
- Operating Ambient Temperature Range: −10 to +60°C
- Luminance Input Resistance (pin 1): 100kΩ min
- Colour Difference Input Currents (pins 2, 4 & 6):
  Unclamped 2μA typ.
  During Clamping −0.2 to +0.2mA
- Clamping Pulse Input Current (pin 8): 20μA max.
- Gain of RGB Preamplifiers: 0dB typ.
- Gain DC Adjustment Range: ±3dB typ.
- Error Amplifier Gain (Conductance): 20mA/V typ.
- Feedback Input Currents (pins 11, 13 & 15): 2μA typ.
- Output Current Swing (pins 10, 12 & 14): −4.4 to +4.4mA

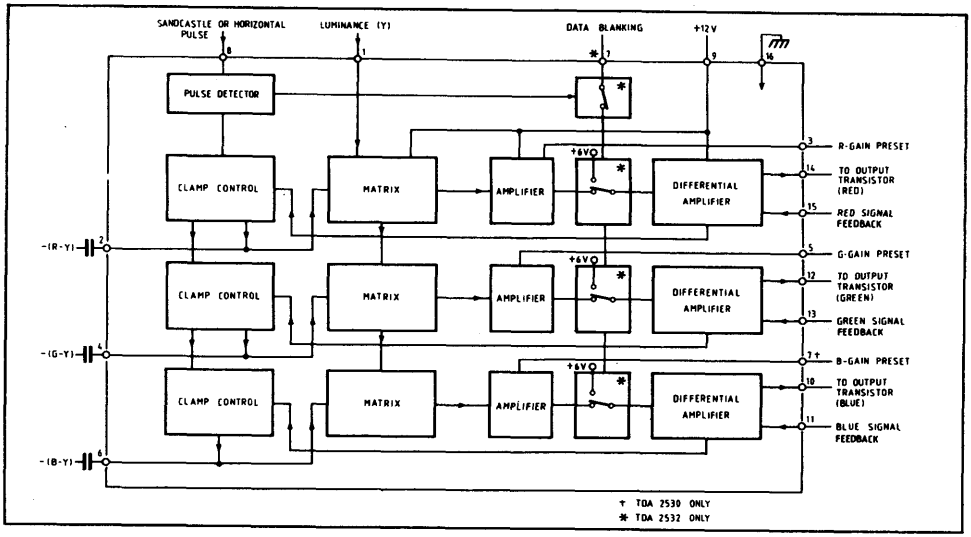

Fig. 2 TDA2530/2 block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Supply voltage (pin 9) = +12V
Luminance input (pin 1) = 1.5V
T_{amb} = +25°C
Measurements refer to pin 16
Test circuit Fig. 3

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Current consumption	9		50		mA	
Luminance input	1					
Black level			1.5		V	
Black-to-white input voltage			1.0		Vp-p	
Input resistance		100			kΩ	
Colour Difference Input						
Input signals						
—(R–Y)	2		1.4		Vp-p	See Note 1
—(G–Y)	4		0.82		Vp-p	
—(B–Y)	6		1.78		Vp-p	
Input currents	2, 4, 6		2	4	μA	
Input currents during clamping	2, 4, 6	±0.2			mA	
Clamp Pulse Input for DC Feedback	8					
Clamping voltage						
ON		7.5		12	V	See Note 2
OFF		0		5.5	V	
Clamping current						
ON				1	μA	
OFF			30		μA	
Feedback Input	11, 13, 15					
DC level during clamping			$0.5V_9$		V	
Gain Adjustment for Colour Drive						
Adjustment voltage range	3, 5, 7	0		10	V	See Note 4
Adjustment voltage for nominal gain	3, 5, 7		5		V	
Nominal gain between colour difference inputs, luminance input and colour feedback inputs	11, 13, 15		0		dB	
Adjustment range of nominal gain	3, 5, 7	±3			dB	$At = \Delta V_{3,5,7,} = \pm 5V$
Differential Amplifier						
Feedback input current	11, 13, 15		2		μA	
Error amplifier gain			20		mA/V	
Output current swing	10, 12, 14		±4.4		mA	
Integrated load resistance	10, 12, 14		680		Ω	See Note 3
Output bias voltage	10, 12, 14		8		V	See Note 3 and applications information
Data blanking (TDA2532 only)	7		≥1		V	Pins 10, 12, 14 go to +6V

NOTES
1. The allocation of —(R–Y), —(G–Y) and —(B–Y) signals to pins 2, 4 and 6 respectively, is not mandatory as all three channels are identical.
2. Switching from clamping ON to OFF occurs at about 6V.
3. The integrated load resistors include series diodes; this means that the resistors can be ignored when V_{10}, V_{12}, $V_{14} > V_9$. Under this condition, external load resistors must be chosen such that the current is nominally 4.4mA. See Fig. 3.
4. The TDA2532 uses pin 7 for data blanking, the gain of one channel is therefore internally preset.

APPLICATIONS INFORMATION (fig 3)

The clamping level, V_{CL} of the video output stages, with set clamping level potentiometers in their mid-positions, is given by:

$$V_{CL} = V_9 \left(1 + \frac{R1}{R2} - \frac{R1}{R3}\right)$$

The gain of the video output stages is given by:

$$\text{Gain} = 1 + \frac{R1}{R2} + \frac{R1}{R3} + \frac{R1}{R4}$$

Attention should be given to earth paths, avoiding common impedances between the input (decoder) side and the output stages.

Printed track area connected to the feedback pins should be kept to a minimum.

To ensure a matched performance of the video output stages, a symmetrical layout of three stages should be employed.

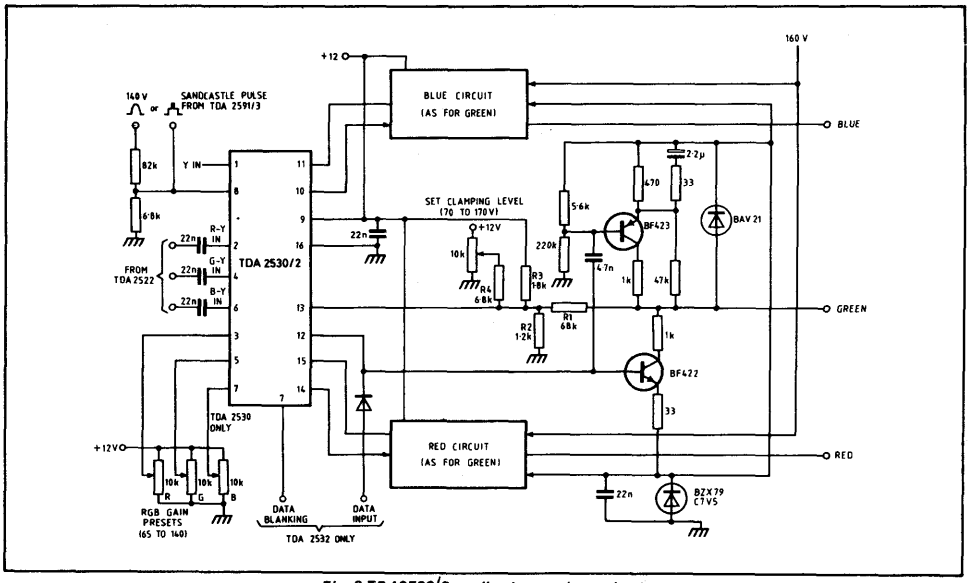

Fig. 3 TDA2530/2 applications and test circuit

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. Luminance signal input.
A 1V black to white positive going luminance input signal is required. Blanking level should be at 1.5V and black level at 1.7V

2. −(R−Y) input signal
The input signal is required to be AC coupled from a low impedance source such as the TDA2522. The coupling capacitor also acts as a clamp capacitor for the TDA2530/2 red output. As the colour difference input impedance is at least 100kΩ, low value coupling capacitors may be used.

3. Red drive adjustment.
A gain variation of the red channel of at least ±3dB about the nominal, is obtained as the DC potential at this pin varies by ±5V about the nominal of 5V. If no connection is made to a gain controlling pin the channel concerned assumes the nominal gain.

4. −(G−Y) input signal (see pin 2)

5. Green drive adjustment (see pin 3)

6. −(B−Y) input signal (see pin 2)

7. TDA2530: Blue drive adjustment (see pin 3)
TDA2532: Data blanking input.
When this pin is taken above 1V the colour output signals on pins 10, 12 and 14 are inhibited, the outputs being clamped to 6V.

8. Clamp pulse input
A positive going line pulse input is required and the pulse should exceed a threshold DC level set by the TDA2530/2 of 7.5 V. An input current of about 0.2mA is required. A maximum current of 1mA should not be exceeded.

9. Positive 12V supply.

10. Blue signal output

11. Blue signal feedback
The signal gain of both the video output stages and IC amplifier are stabilised by the feedback circuits. DC clamping is achieved by sampling of the feedback level during blanking. The black level potentials at the collectors of the video output stages may be varied independently by adjustable DC current sources applied to the feedback input pins. The DC levels at these pins are such that the feedback resistor and a resistor network between the 12V supply and earth provide a potential of 6V during blanking.

12. Green signal output

13. Green signal feedback (see pin 11)

14. Red signal output

15. Red signal feedback (see pin 11)

16. Negative supply (earth)

ABSOLUTE MAXIMUM RATINGS

Voltages	
Supply voltage (V_9)	15V
Pin 1, 2, 3, 4, 5, 6 & 7	0V to V_9
Pin 8	V_9
Pin 10	V_9 to V_9 + 3V
Pin 12	V_{13} to V_9 + 3V
Pin 14	V_{15} to V_9 + 3V
Pins 11, 13 and 15	0.3V_9 to V_9
Current	
Pin 8	1mA
Thermal	
Total power dissipation	1W
Storage temperature	−55°C to +125°C
Operating ambient temperature	−10°C to +60°C

PLESSEY
Semiconductors

TDA2540 TDA2541

TELEVISION IF AMPLIFER AND DEMODULATOR
(TDA2540 for NPN tuners, TDA2541 for PNP tuners)

The TDA2540 and TDA2541 are IF amplifier and demodulator circuits for colour and monochrome television receivers using NPN and PNP tuners respectively. The two circuits are in other respects identical. A VCR switch is incorporated for switching off the video signal when inserting a VCR playback signal.

FEATURES

- Gain-Controlled Wideband Amplifier, Providing Complete IF Gain
- Synchronous Demodulator
- White Spot Inverter
- Video Preamplifier with Noise Protection
- DC Controlled AFC
- AGC Circuit with Noise Gating
- Tuner AGC Output
- VCR Switch

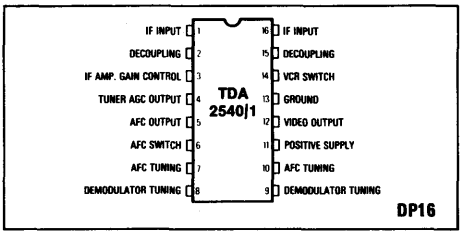

Fig. 1 Pin connections (top view)

QUICK REFERENCE DATA

- Supply Voltage (pin 11): 12V typ.
- Supply Current: 50mA typ.
- IF Input Voltage at f = 38.9MHz (pins 1 & 16): 100μV RMS typ.
- Video Output Voltage (pin 12): 3V typ.
- IF Voltage Gain Control Range: 64dB typ.
- Signal-to-noise Ratio at V_{in} = 10mV: 58dB typ.
- AFC O/P Voltage Swing for Δf = 100kHz (pin 6): 10V min.

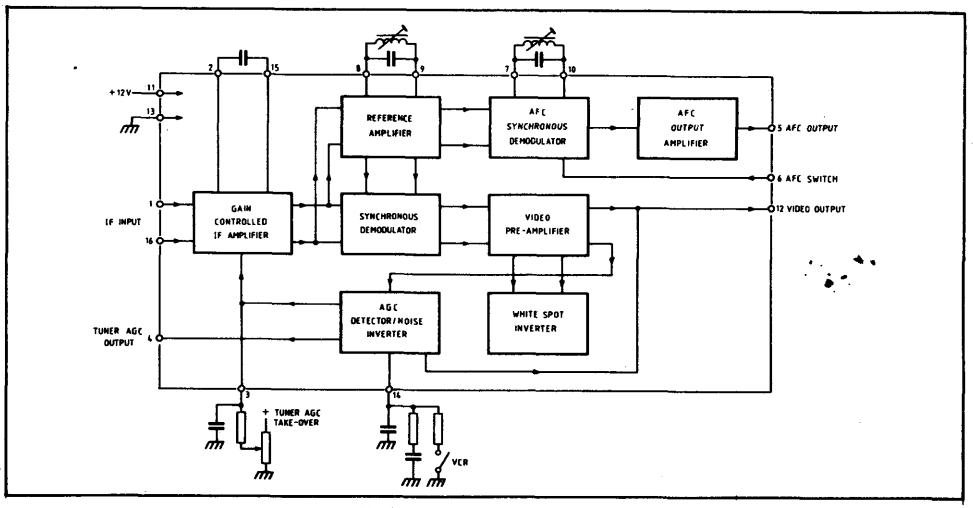

Fig. 2 TDA2540/TDA2541 block diagrams

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage (pin 11) = 12V
T_{amb} = +25°C
Measurements referred to pin 13
Test circuits Figs. 9 & 10

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply Current			50		mA	
Supply voltage range	11	10.2	12	13.8	V	
IF input voltage for onset of AGC	1–16		100	150	μV RMS	f = 38.9 MHz
Differential input impedance	1–16		2//2		kΩ// pF	
Zero-signal output level	12	5.7	6.0	6.3	V	
Top sync. output level	12	2.9	3.07	3.2	V	
AFC output voltage swing	6	10	11		V	Δ f = 100kHz
IF voltage control range			64		dB	
Signal-to-noise ratio			58		dB	V_{in} = 10mV, See Note 1
Video amplifier 3dB bandwidth			6		MHz	
Differential gain			4	10	%	
Differential phase			2	10	deg.	
Carrier signal at video output			4	30	mV	
2nd harmonic of carrier at video output			20	30	mV	
Change of frequency at AFC output voltage swing of 10V			100	200	kHz	
Intermodulation at 1.1MHz						
Blue		46	60		dB	See Note 2 and Figs 3 and 4
Yellow		46	50		dB	
Intermodulation at 3.3MHz		46	54		dB	
AFC switches off at:	6			2.5	V	
VCR switches off at	14			1.1	V	
White spot inverter threshold			6.6		V	
White spot insertion level			4.7		V	See Fig 5
Noise inverter threshold level			1.8		V	
Noise insertion level			3.8		V	
Typical tuner AGC output current	4	0		10	mA	
Tuner AGC output voltage	4			0.3	V	I_4 = 10mA
Tuner AGC output leakage current	4			15	μA	V_{14} = 3V, V_4 = 12V

NOTES:

1. $S/N = \frac{V_{out}\ \text{black-to-white}}{V_{in}\ \text{at bandwidth} = 5MHz}$

2. Intermodulation at 1.1MHz = $20 \log \frac{V_{out}\ \text{at 4.4MHz}}{V_{out}\ \text{at 1.1MHz}}$

3. Intermodulation at 3.3MHz = $20 \log \frac{V_{out}\ \text{at 4.4MHz}}{V_{out}\ \text{at 3.3MHz}}$

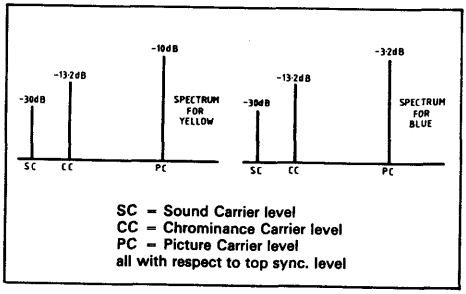

Fig. 3 Input conditions for intermodulation measurements – standard colour bar with 75 percent contrast

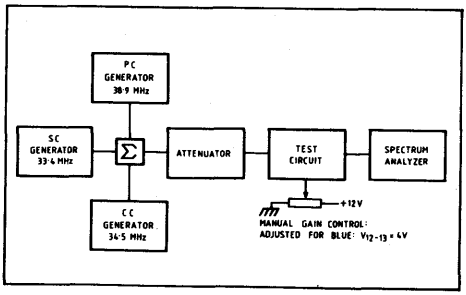

Fig. 4 Test set-up for intermodulation

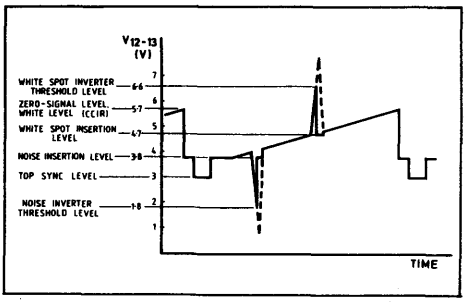

Fig. 5 Video output waveform showing white spot and noise inverter threshold levels

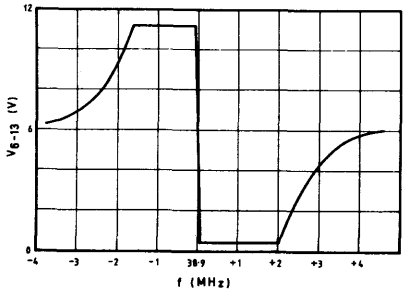

Fig.6 AFC output voltage (pin 5) as a function of frequency

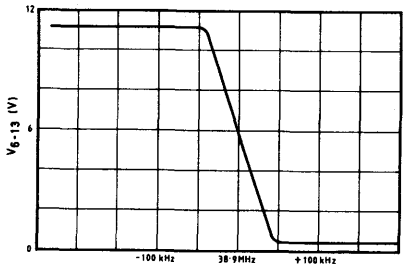

Fig. 7 Expansion of Fig. 6

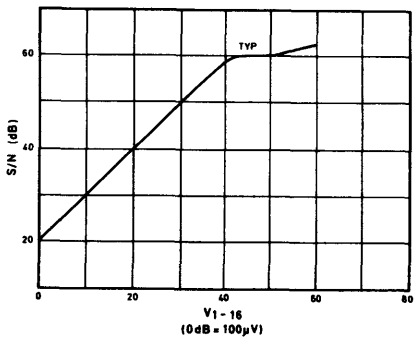

Fig. 8 Signal-to-noise ratio as a function of input voltage

APPLICATIONS INFORMATION

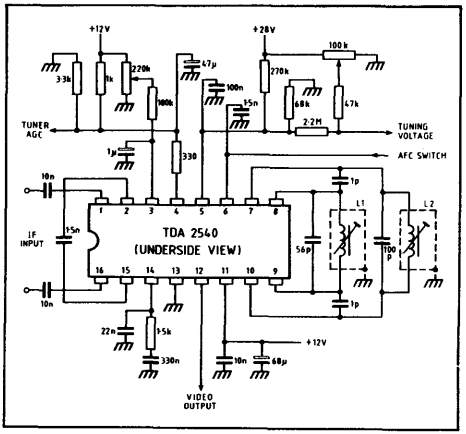

Fig. 9 TDA2540 typical application circuit

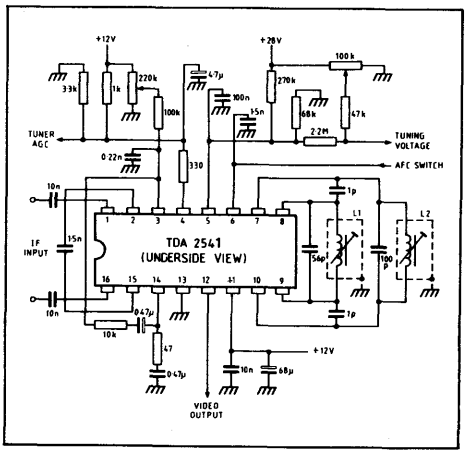

Fig. 10 TDA2541 typical application circuit

ABSOLUTE MAXIMUM RATINGS

Supply voltage	13.8V
Tuner AGC voltage	12V
Storage temperature	−55°C to +125°C
Operating ambient temperature	−10°C to +60°C

PLESSEY
Semiconductors

TDA2560

LUMINANCE AND CHROMINANCE CONTROL COMBINATION

The TDA2560 is an integrated circuit for use in colour television receiver decoding systems, and consists of a luminance amplifier and a chrominance amplifier. The luminance amplifier has a low input impedance so that luminance delay line matching is very easy. The chrominance amplifier has a combined chroma and burst output, the burst signal amplitude unaffected by contrast and saturation control.

QUICK REFERENCE DATA

- Supply Voltage (pin 8) 12V typ.
- Supply Current 45mA typ.
- Luminance Signal Input Current (Black-to-White Value) (pin 14) 0.2mA typ.
- Chrominance Input Signal (pins 2 & 1) 4 to 80 mVp-p
- Luminance Output Signal at Nominal Contrast (Black-to-White Value) (pin 10) 3V typ.
- Chrominance Output Signal at Nominal Contrast and Saturation and 1.25Vp-p Burst Output (pin 6) 2.5Vp-p typ.
- Contrast Control Range >20dB
- Saturation Control Range >20dB

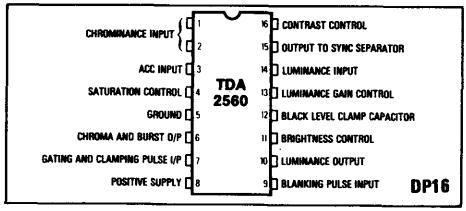

Fig. 1 Pin connections (top view)

FEATURES

Luminance Amplifier

- DC Contrast Control
- DC Brightness Control
- Black Level Clamp
- Blanking
- Additional Video O/P with +ve Sync.

Chrominance Amplifier

- Gain Control Amplifier
- Chrominance Gain Control Tracked with Contrast Control
- Separate DC Saturation and Contrast Controls
- Direct Delay Line Drive

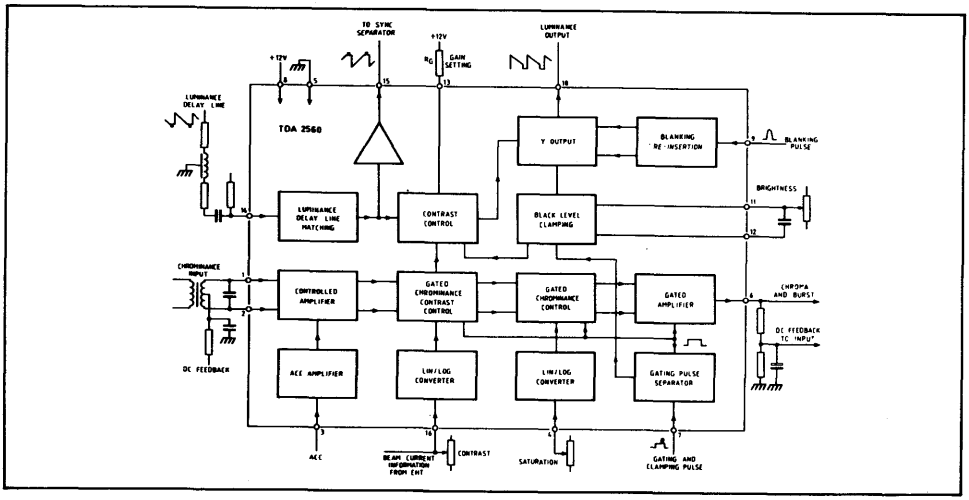

Fig. 2 TDA2560 block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Supply voltage (pin 8) = +12V
T_{amb} = +25°C
Gain setting resistor, R_G, (pin 13) = 2.7kΩ
Measurements referred to pin 5
Test circuit Fig. 5

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage range	8	10	12	14	V	
Supply current	8		45		mA	Load on pin 6 = 1.5kΩ no load on pins 10 and 15
Permitted supply line hum	8			100	mAp–p	
Luminance Amplifier						
Input signal current	14		0.2		mA	Black-to-white value
Input bias current	14		0.25		mA	
Input impedance	14		150		Ω	Input bias current = 0.25mA
Gain	13					See operating Note 1
Contrast control range		20			dB	
Contrast control voltage range	16					See Fig. 3
Contrast control current	16			8	µA	
Black level range	10	1		3	V	
Typical brightness control voltage range	11	1		3	V	
Brightness control current	11			20	µA	$V_{11} > 4V$
Black level temperature stability			0.1		mV/°C	
Black level stability when changing contrast						See functional description (pin 10)
Bandwidth (–3dB)		5			MHz	At nominal contrast (Max contrast setting –3dB)
Output voltage	10		3		V	Black-to-white value
Output to sync separator	15		3.4		Vp–p	I_{14} = 0.2mA black-to-white
Black level clamp pulse	7					See Operating Note 2
ON		7		V_8	V	
OFF				5	V	
Blanking pulse	9					See Operating Note 3
ON		2.5		4.5		For 0V on pin 10
OFF				1.5	V	
ON		6		V_8	V	For 1.5V on pin 10
OFF				4.5	V	
Chrominance Amplifier						See note 1
Input signal	2–1	4		80	mVp–p	
Chrominance output signal at nominal contrast and saturation level	6		2		Vp–p	See note 2
Max, chrominance output	6		4.6		V	
Bandwidth (–3dB)			6		MHz	
Ratio of burst and chrominance at nominal contrast and saturation						See Operating Notes 4 and 5
ACC starting voltage	3		1.2		V	See Operating Note 6
ACC range		30			dB	
Tracking between luminance and chrominance with contrast control			±1		dB	10dB control
Saturation control range		20			dB	
Saturation control voltage range	4					See Fig. 4
Gating pulse	7					
ON		2.3		5	V	
OFF				1	V	
Width		8			µs	
Signal-to-noise ratio		46			dB	
Phase shift between burst and chrominance				5	deg	

NOTES:
1. All figures for the chrominance signals are based on a colour bar signal with 75 per cent saturation: i.e. burst-to-chrominance ratio is 1:2.
2. At a burst signal of 1V peak-to-peak: see also Operating Notes 4 and 5.

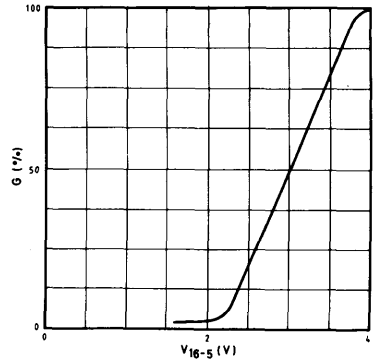

Fig. 3 Contrast control of luminance and chrominance amplifier

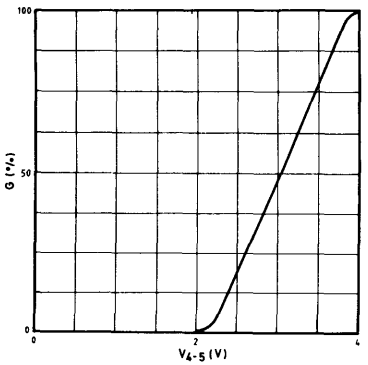

Fig. 4 Saturation control of chrominance amplifier

FUNCTIONAL DESCRIPTION

Functions listed by pin number.

1. and 2. Balanced chrominance input signal
This is derived from the chrominance signal bandpass filter, designed to provide a push-pull input. A signal amplitude of at least 4mV peak-to-peak is required between pins 1 and 2. The chrominance amplifier is stabilized by an external feedback loop from the output (pin 6) to the input (pins 1 and 2). The required level at pins 1 and 2 will be 3V.

3. ACC input
A negative-going potential, starting at +1.2V, gives a 40dB range of ACC. Maximum gain reduction is achieved at an input voltage of 500mV.

4. Chrominance saturation control
A control range of +6dB to —14dB is provided over a range of DC potential on pin 4 from +2 to +4V. The saturation control is a linear function of the control voltage.

5. Negative supply (ground)

6. Chrominance signal output
For nominal settings of saturation and contrast controls (max. — 6dB for saturation, and max. —3dB for contrast) both the chroma and burst are available at this pin, and in the same ratio as at the input pins 1 and 2. The burst signal is not affected by the saturation and contrast controls. The ACC circuit of the TDA2522 will hold the colour burst amplitude constant at the input of the TDA2522. As the PAL delay line is situated here between the TDA2560 and TDA2522 there may be some variation of the nominal 1V peak-to-peak burst output of the TDA2560, according to the tolerances of the delay line. An external network is required from pin 6 of the TDA2560 to provide DC negative feedback in the chroma channel via pins 1 and 2.

7. Burst gating and clamping pulse input
A two-level pulse is required at this pin to be used for burst gate and black level clamping. The black level clamp is activated when the pulse level is greater than 7V. The timing of this interval should be such that no appreciable encroachment occurs into the sync pulse on picture line periods during normal operation of the receiver. The burst gate, which switches the gain of the chroma amplifier to maximum, requires that the input pulse at pin 7 should be sufficiently wide (at least 8μs) at the actuating level of 2.3V.

8. +12V power supply
Correct operation occurs within the range 10 to 14V. All signal and control levels have a linear dependency on supply voltage but, in any given receiver design, this may be restricted due to consideration of tracking between the power supply variations and picture contrast and chroma levels.

9. Flyback blanking input waveform
This pin is used for blanking the luminance amplifier. When the input pulse exceeds the +2.5V level, the output signal is blanked to a level of about 0V. When the input exceeds a +6V level, a fixed level of about 1.5V is inserted in the output. This level can be used for clamping purposes.

10. Luminance signal output
An emitter follower provides a low impedance output signal of 3V black-to-white amplitude at nominal contrast setting having a black level in the range 1 to 3V. An external emitter load resistor is not required.
The luminance amplitude available for nominal contrast may be modified according to the resistor value from pin 13 to the +12V supply. At an input bias current I_{14} of 0.25mA during black level the amplifier is compensated so that no black level shift more than 10V occurs at contrast control. When the input current deviates from the quoted value the black level shift amounts to 100mV/mA.

11. Brightness control
The black level at the luminance output (pin 10) Is identical to the control voltage required at this pin. A range of black level from 1 to 3V may be obtained.

12. Black level clamp capacitor

13. Luminance gain setting resistor
The gain of the luminance amplifier may be adjusted by selection of the resistor value from pin 13 to +12V. Nominal luminance output amplitude is then 3V black-to-white at pin10 when this resistor is 2.7kΩ and the input current is 0.2mA black-to-white. Maximum and minimum values of this resistor are 3.9kΩ and 1.8kΩ.

14. Luminance signal input
A low input impedance in the form of a current sink is obtained at this pin. Nominal input current is 0.2mA

black-to-white. The luminance signal may be coupled to pin 14 via a DC blocking capacitor and, in addition, a resistor employed to give a DC current into pin 14 at black level of about 0.25mA. Alternatively DC coupling from a signal source such as the TDA2541 may be employed.

15. Luminance signal output for sync separator purposes

A luminance signal output with positive-going sync is available which is not affected by the contrast control or the value of resistor at pin 13. This voltage is intended for drive of sync separator circuits. The output amplitude is 3.4V peak-to-peak when the luminance signal input is 0.2mA black-to-white.

16. Contrast control

With 3V on this pin the gain of the luminance channel is such that 0.2mA black-to-white at pin 14 gives a luminance output on pin 10 of 3V black-to-white. The nominal value of 2.7k Ω is then assumed for the resistor from pin 13 to the +12V supply. The variation of control potential at pin 16 from 2 to 4V gives —17 to +3dB gain variation of the luminance channel. A similar variation in the chrominance channel occurs in order to provide correct tracking between the two signals.

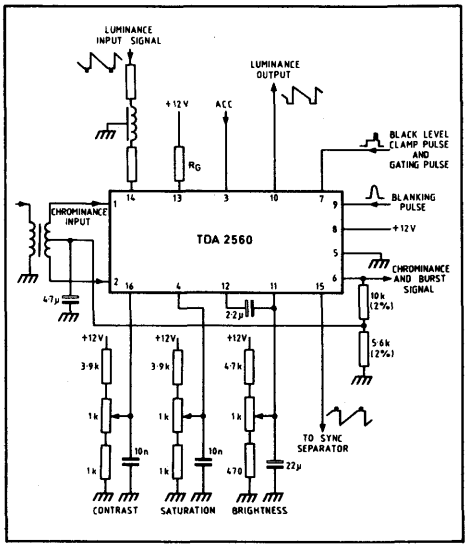

Fig. 5 Application and test circuit

ABSOLUTE MAXIMUM RATINGS

Supply voltage	14V
Total power dissipation	930mW
Storage temperature	—55°C to +125°C
Operating ambient temperature	—10°C to +65°C

OPERATING NOTES

1. The gain of the luminance amplifier can be adjusted by setting the gain of the contrast control circuit with selection of the discrete resistor R_G (see Fig. 5). This circuit configuration has been chosen to reduce the spread of the gain to a minimum (main cause of spread is the spread of the ratio of the delay line matching resistors and the resistor R_G). At R_G = 2.7k Ω the output voltage at nominal contrast (maximum —3dB) is 3V black-to-white for an input current 0.2mA black-to-white.
2. The pulse applied to pin 7 is used for gating of the chrominance amplifier and black level clamping. The latter function is actuated at a +7V level. The input pulse must have such an amplitude that the clamping circuit is active only during the back porch of the blanking interval. The gating pulse switches the gain of the chroma amplifier to maximum during the flyback time, when the pulse rises above 2.3V and switches it back to normal setting when the pulse falls below 1V.
3. The blanking pulse (pin 9) is used for blanking the luminance amplifier. When the pulse exceeds the 2.5V level the output signal is blanked to a level of about 0V. When the input exceeds a +6V level a fixed level of typ. +1.5V is inserted in the output signal. This level can be used for clamping purposes.
4. The chrominance and burst signal are both available on pin 6. The burst signal is not affected by the contrast and saturation control and is kept constant by the ACC circuit of the TDA2522. The output of the delay line matrix circuit, which is the input of the TDA2522, is thus automatically compensated for the insertion losses. This means that the output signal of the TDA 2560 is determined by the insertion losses of the delay line. At nominal contrast and saturation setting the ratio of burst to chrominance signal at the output is typically indentical to that at the input.
5. Nominal contrast is specified as maximum contrast —3dB. Nominal saturation is specified as maximum saturation —6dB.
6. A negative-going control voltage gives a decrease in gain.

PLESSEY
Semiconductors

TDA2590

LINE OSCILLATOR COMBINATION

The TDA2590 is an integrated line oscillator circuit for colour television receivers using thyristor or transistor line deflection output stages.

The circuit incorporates a line oscillator which is based on the threshold switching principle, a line deflection output stage capable of direct drive of thyristor deflection circuits, phase comparison between the oscillator voltage and both the sync pulse and line flyback pulse. Also included on the chip is a switch for changing the filter characteristic and the gate circuit when used for VCR.

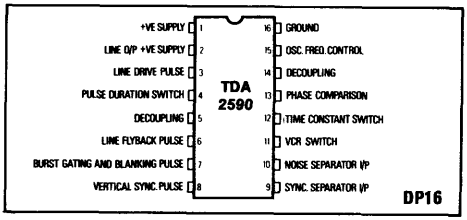

Fig. 1 Pin connections (top view)

FEATURES

- Coincidence Detector
- Sync Separator
- Noise Separator
- Vertical Sync Separator
- Colour Burst Keying
- Line Flyback Pulse Generator
- Output Pulse Phase Shifter
- Output Pulse Duration Switching
- Sync Gating Pulse Generator
- Low Supply Voltage Protection

QUICK REFERENCE DATA

- Supply Voltage (pin 1) 12V typ.
- Supply Current 30mA typ.
- Sync Separator Input (pin 9) 3V p-p typ.
- Pulse Duration Switch Input (pin 4)
  at $t = 6\mu s$ 9.4V to V_1
  at $t = 14\mu s + t_d$ 0V to 4V
- VCR Switch ON (pin 11) 0V to 1.5V and 9V to V_1

Output signal

- Vertical Sync Pulse (pin 8) 11V p-p (typ.)
- Burst Gating Pulse (pin 7) 11V p-p (typ.)
- Line Drive Pulse (pin 3) 10.5V p-p (typ.)

ABSOLUTE MAXIMUM RATINGS

Voltages	
Supply pin 1 (when supplied by the IC)	13.2V
Supply pin 2	18V
Pin 4	0V to 13.2V
Pin 9	−6V to +6V
Pin 10	−6V to +6V
Pin 11	0V to 13.2V
Currents	
Pin 2	400mA peak
Pin 3	400mA peak
Pin 4	1mA peak
Pin 6	10mA peak
Pin 7	10mA peak
Pin 11	2mA peak
Power dissipation	
Total power dissipation	800mW
Temperature	
Storage temperature	−55°C to +125°C
Operating ambient temperature	−10°C to +60°C

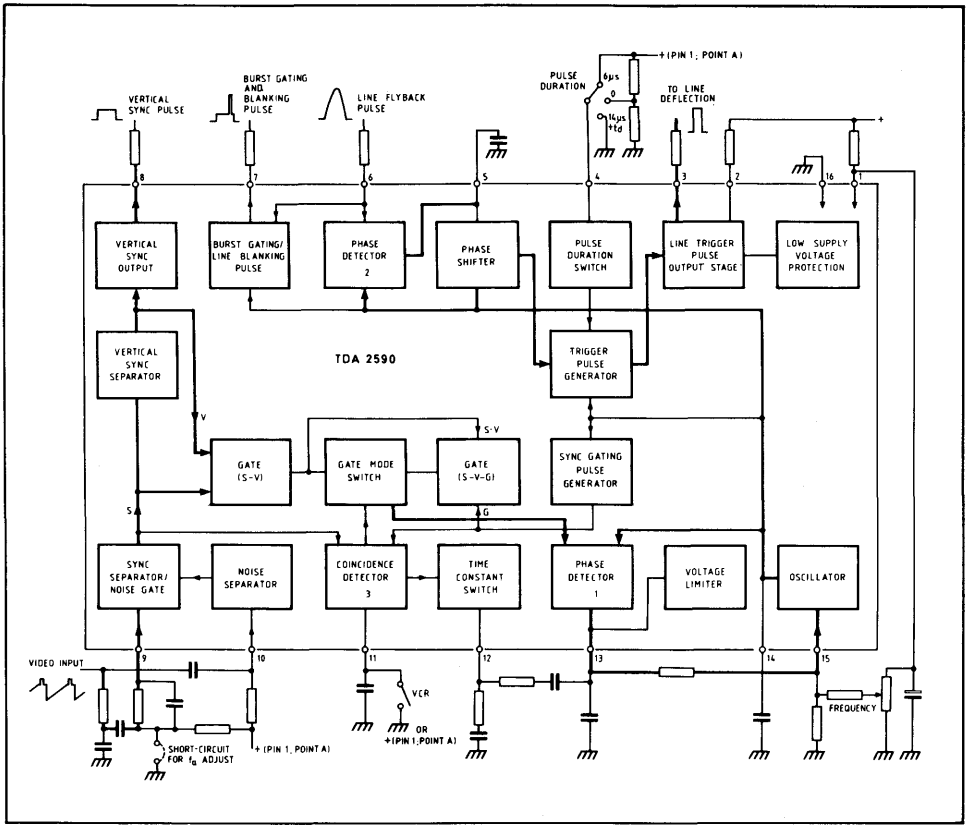

Fig. 2 TDA2590 block diagram

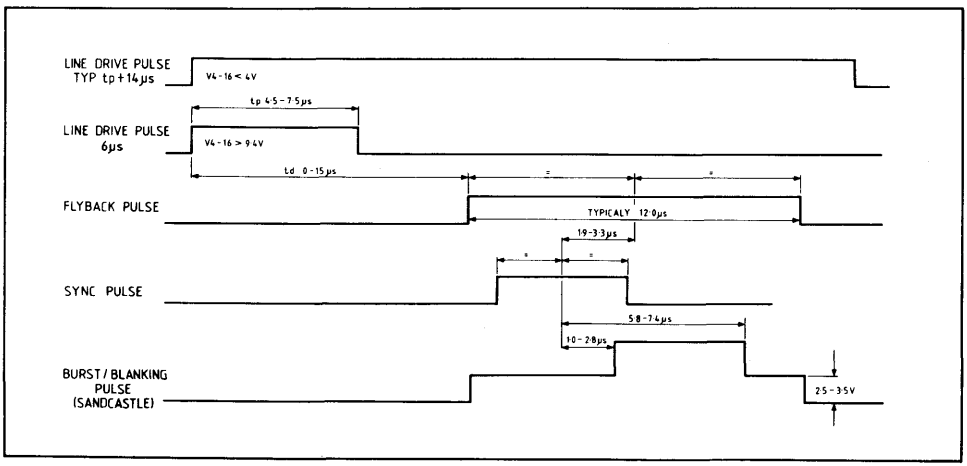

Fig. 3 TDA2590 timing relationships

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_1 = 12V$
$T_{amb} = +25°C$
Refer to timing diagram, Fig. 3 and Application circuit, Fig. 4
Voltages are referred to pin 6

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Sync separator	9					
Input switching voltage			0.8		V	
Input keying current		5		100	µA	
Input blocking current				1	µA	$V_9 = -5V$
Input switching current				5	µA	
Noise separator	10					
Input switching voltage			1.4		V	
Input keying current		5		100	µA	
Input switching current			150		µA	
Input blocking current				1	µA	$V_{10} = -5V$
Line flyback pulse	6					
Input current		10			µA	
Input switching voltage			1.4		V	
Input limiting voltage		−0.7		+1.4	V	
Input resistance			400		Ω	
Pulse duration switch	4					
Input voltage		9.4		V_1	V	$t = 6µs$
Input current		200			µA	
Input voltage		0		4.0	V	$t = 14µs + t_d$
Input current		200			µA	
Input voltage		5.4		6.5	V	$t = 0, V_3 = 0$
Input current (input open)			0		µA	See note 1
VCR switch	11					
Input voltage (typical range)		0		1.5	V	See note 2
		9		V_1	V	
Input current		200			µA	$V_{11} = 0V$ to 1.5V
Output current		1		2	mA	$V_{11} = 9V$ to V_1
Vertical sync pulse (positive going)	8					
Output voltage		10	11		Vp–p	
Output resistance			2		kΩ	
Burst gating pulse (positive-going)	7					
Output voltage		10	11		Vp–p	
Output resistance			400		Ω	
Blanking pulse	7					
Output voltage (typical range)		2.5		3.5	Vp–p	
Output resistance			400		Ω	
Line drive pulse (positive going)	3					
Output voltage			10.5		Vp–p	
Output current (average value)			100		mA	
Output resistance for leading edge of line pulse			2.5		Ω	
Output resistance for trailing edge of line pulse			20		Ω	
Oscillator	14					
Threshold voltage low level			4.4		V	
Threshold voltage high level			7.6		V	
Discharge current			0.47		mA	
Phase comparison ($ø_1$: sync pulse/oscillator)	13					
Control voltage range (typ)		3.8		8.2	V	
Control current		1.9	2.1	2.3	mAp–p	
Output blocking current				1	µA	$V_{13} = 4V$ to 8V
Output resistance		High (see note 3)				$V_{13} = 4V$ to 8V
		Low (see note 4)				$V_{13} < 3.8V$ or $> 8.2V$
Time constant switch	12					
Output voltage			6		V	
Output current				1	mA	
Output resistance			100		Ω	$V_{11} = 2.5V$ to 7V
			60		kΩ	$V_{11} < 1.5V$ or $> 9V$

ELECTRICAL CHARACTERISTICS (Contd.)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Coincidence detector (ϕ_3)	11					
Output voltage typical range		0.5		6	V	
Output current:						
without coincidence			0.1		mAp–p	
with coincidence			0.5		mAp–p	
Phase comparison (ϕ_2: oscillator/ line flyback pulse)	5					
Control voltage range (typ)		5.4		7.6	V	
Control current			1		mAp–p	
Output resistance		High (see note 3)				$V_5 = 5.4V$ to $7.6V$
			8		kΩ	$V_5 < 5.4V$ or $> 7.6V$
Input current at blocked phase detector				5	µA	$V_5 = 5.4V$ to $7.6V$
Applications (see Fig. 4)	9					
Sync separator						
Input voltage (negative video signal)		1	3	7	Vp–p	
Input keying current range		5		100	µA	
Noise gating	10					
Input voltage		1	3	7	Vp–p	
Input keying current range		5		100	µA	
Superimposed noise voltage				7	Vp–p	
Vertical sync pulse separator						
Delay between leading edge of input and output signal, t_{on}			12		µs	
Delay between trailing edge of input and output signal, t_{off}				t_{on}	µs	
Output voltage	8		11		Vp–p	
Output resistance	8		2		kΩ	
Oscillator						
Frequency: free running			15.625		kHz	$C_{14} = 4.7nF$, $R_{15} = 10k\Omega$
Spread of frequency, $\Delta f_o/f_o$				±5	%	See note 5
Frequency control sensitivity, $\Delta f_o/\Delta I_{15}$			31		Hz/µA	
Adjustment range of network in Fig. 2			±10		%	
Influence of supply voltage on frequency $\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$				±0.05		See note 5, $V_1 = 12V$
Change of frequency when V_1 drops to 5V				±10	%	See note 5
Temperature coefficient of oscillator frequency per °C				$\pm 10^{-4}$		
Phase comparison (ϕ_1: sync pulse/oscillator)						
Control sensitivity			2		kHz/µs	
Catching and holding range (82kΩ between pins 13 and 15)			±780		Hz	$R_{13-15} = 82k\Omega$
Spread of catching and holding range			±10		%	See note 5
Phase comparison (ϕ_2: oscillator/ line flyback pulse)						
Permissible delay between leading edge of output pulse and leading edge of flyback pulse, Δtd		0		15	µs	
Static control error, td/td				0.2	%	
Overall phase relation See Note 6						
Phase relation between middle of sync pulse and the middle of the flyback pulse, t			2.6		µs	
Tolerance of phase relation Δt				0.7	µs	
Adjustment sensitivity of overall phase relation	5					
caused by: adjustment voltage $\Delta V_5/\Delta t$			0.1		V/µs	
adjustment current, $\Delta I_5/\Delta t$			30		µA/µs	

ELECTRICAL CHARACTERISTICS (Contd.)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Burst gating pulse						
Phase relation between middle of sync pulse at the input and the trailing edge of the burst gating pulse	7	5.8	6.6	7.4	µs	At 7V level
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse	7	1.0	1.9	2.8	µs	$V_7 = 7V$ At 7V level
Line drive pulse						
Output pulse duration, t_p for thyristor O/P	3	4.5	6.0	7.5	µs	$V_4 > 9.4V$
Output pulse duration, t_p for transistor O/P	3		14 + t_d		µs	$V_4 < 4V$, see note 7
Supply voltage for switching off the output pulse	1		4		V	
Internal gating pulse						
Pulse duration			7.5		µs	

NOTES
1. May also be left unconnected
2. VCR 'on' is normally achieved by connecting pins 11, via the VCR switch, to either ground or V_1
3. Current source
4. Emitter follower
5. Excluding external component tolerances
6. The adjustment of the overall phase relation and consequently the leading edge of the output pulse occurs automatically by phase detector 2 (see Fig. 2)
7. t_d = switch-off delay of line output stage.

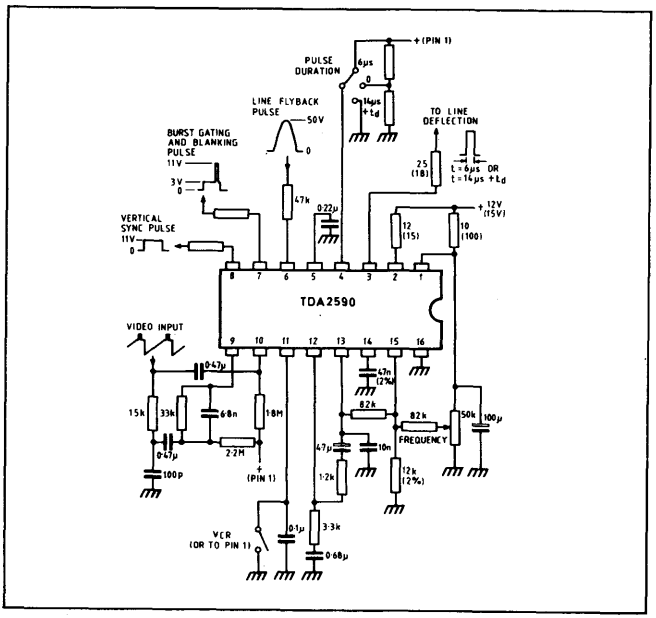

Fig. 4 Application and test circuit

PLESSEY
Semiconductors

TDA2591/3

LINE OSCILLATOR COMBINATION

The TDA2591 and TDA2593 are integrated line oscillator circuits for colour television receivers using thyristor or transistor line deflection output stages.

The circuits incorporate a line oscillator which is based on the threshold switching principle, a line deflection output stage capable of direct drive of thyristor deflection circuits, phase comparison between the oscillator voltage and both the sync pulse and line flyback pulse. Also included on the chip is a switch for changing the filter characteristic and the gate circuit when used for VCR.

The TDA2593 generates a sandcastle pulse (at pin 7) suitable for use with the TDA2532.

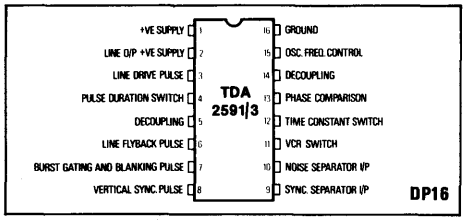

Fig.1 Pin connections (top view)

FEATURES

- Coincidence Detector
- Sync Separator
- Noise Separator
- Vertical Sync Separator
- Colour Burst Keying
- Line Flyback Pulse Generator
- Output Pulse Phase Shifter
- Output Pulse Duration Switching
- Sync Gating Pulse Generator
- Low Supply Voltage Protection

QUICK REFERENCE DATA

- Supply Voltage (pin 1) 12V typ.
- Supply Current 30mA typ.
- Sync Separator Input (pin 9) 3V p-p typ.
- Pulse Duration Switch Input (pin 4)
  at $t = 7\mu s$ 9.4V to V_1
  at $t = 14\mu s + t_d$ 0V to 4V
- VCR Switch ON (pin 11) 0V to 1.5V and 9V to V_1

Output signal

- Vertical Sync Pulse (pin 8) 11V p-p (typ.)
- Burst Gating Pulse (pin 7) 11V p-p (typ.)
- Line Drive Pulse (pin 3) 10.5V p-p (typ.)

ABSOLUTE MAXIMUM RATINGS

Voltages		
Supply pin 1 (when supplied by the IC)	13.2V	
Supply pin 2	18V	
Pin 4	0V to 13.2V	
Pin 9	−6V to +6V	
Pin 10	−6V to +6V	
Pin 11	0V to 13.2V	
Currents		
Pin 2	400mA peak	} 650mA thyristor drive only
Pin 3	400mA peak	
Pin 4	1mA peak	
Pin 6	10mA peak	
Pin 7	10mA peak	
Pin 11	2mA peak	
Power dissipation		
Total power dissipation	800mW	
Temperature		
Storage temperature	−55°C to +125°C	
Operating ambient temperature	−10°C to +60°C	

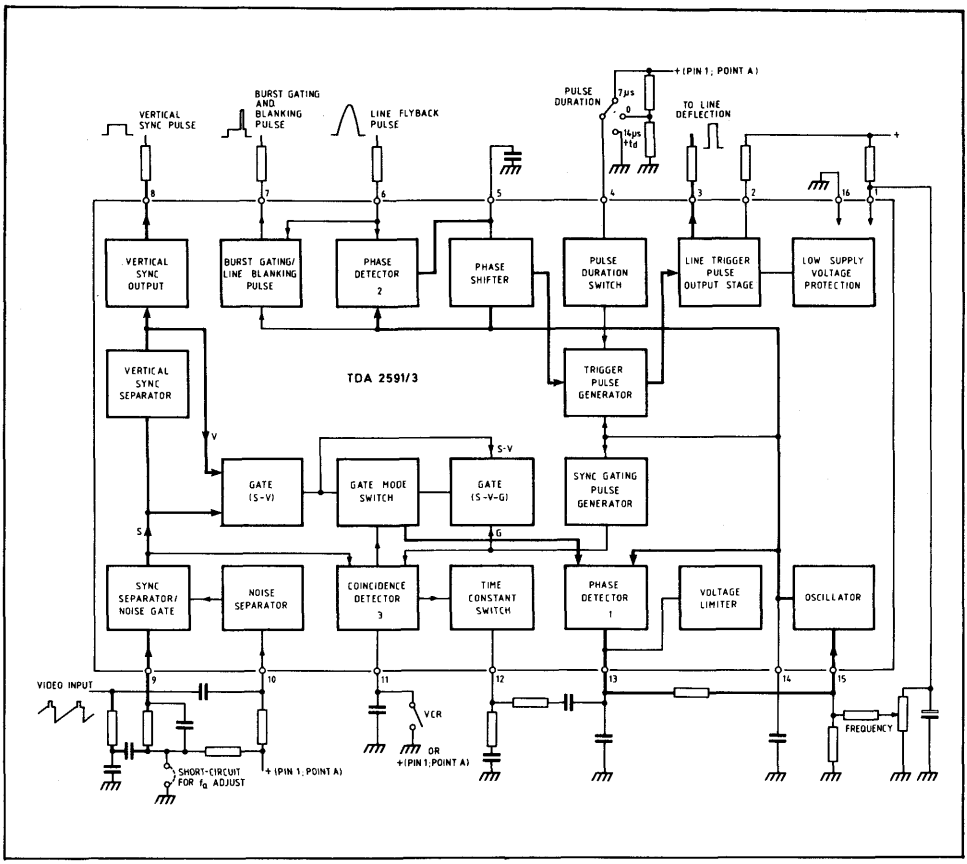

Fig. 2 TDA2591/3 block diagram

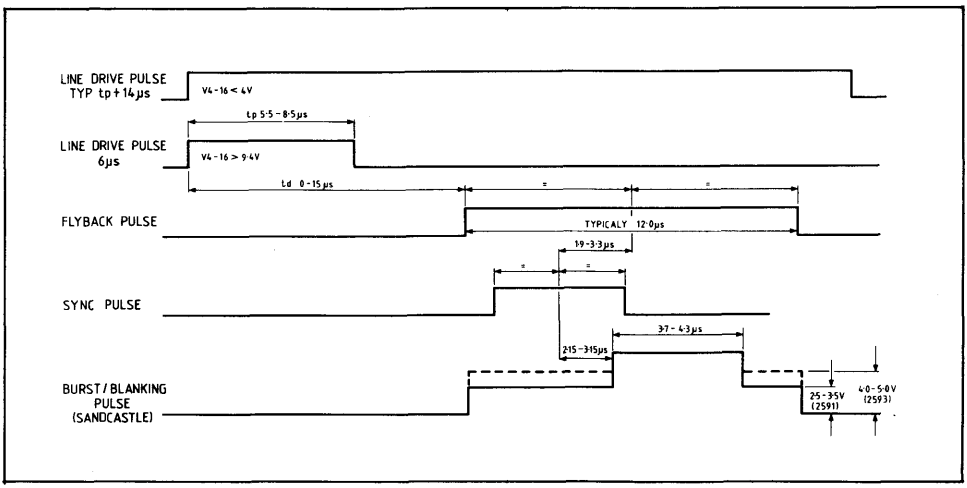

Fig. 3 TDA2591/3 timing relations

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_1 = 12V$
$T_{amb} = +25°C$
Refer to timing diagram, Fig. 3 and Application circuit, Fig. 4
Voltages are referred to pin 6

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Sync separator	9					
Input switching voltage			0.8		V	
Input keying current		5		100	μA	
Input blocking current				1	μA	$V_9 = -5V$
Input switching current				5	μA	
Noise separator	10					
Input switching voltage			1.4		V	
Input keying current		5		100	μA	
Input switching current			150		μA	
Input blocking current				1	μA	$V_{10} = -5V$
Line flyback pulse	6					
Input current		10			μA	
Input switching voltage			1.4		V	
Input limiting voltage		−0.7		+1.4	V	
Input resistance			400		Ω	
Pulse duration switch	4					
Input voltage		9.4		V_1	V	$t = 7\mu s$
Input current		200			μA	
Input voltage		0		4.0	V	$t = 14\mu s + t_d$
Input current		200			μA	
Input voltage		5.4		6.5	V	$t = 0, V_3 = 0$
Input current (input open)			0		μA	See note 1
VCR Switching	11					
Input voltage (typical range)		0		1.5	V	See note 2
		9		V_1	V	
Input current		200			μA	$V_{11} = 0V$ to 1.5V
Output current		1		2	mA	$V_{11} = 9V$ to V_1
Vertical sync pulse (positive going)	8					
Output voltage		10	11		Vp–p	
Output resistance			2		kΩ	
Burst gating pulse (positive-going)	7					
Output voltage		10	11		Vp–p	
Output resistance			400		Ω	
Blanking pulse	7					
Output voltage (typical range) 2591		2.5		3.5	Vp–p	
Output voltage (typical range) 2593		4.0		5.0	Vp–p	
Output resistance			400		Ω	
Line drive pulse (positive going)	3					
Output voltage			10.5		Vp–p	
Output current (average value)			100		mA	
Output resistance for leading edge of line pulse			2.5		Ω	
Output resistance for trailing edge of line pulse			20		Ω	
Oscillator	14					
Threshold voltage low level			4.4		V	
Threshold voltage high level			7.6		V	
Discharge current			0.47		mA	
Phase comparison ($ø_1$: sync pulse/oscillator)	13					
Control voltage range (typ)		3.8		8.2	V	
Control current		1.9	2.1	2.3	mAp–p	
Output blocking current				1	μA	$V_{13} = 4V$ to 8V
Output resistance		High (see note 3)				$V_{13} = 4V$ to 8V
		Low (see note 4)				$V_{13} < 3.8V$ or $> 8.2V$
Time constant switch	12					
Output voltage			6		V	
Output current				1	mA	
Output resistance			100		Ω	$V_{11} = 2.5V$ to 7V
			60		kΩ	$V_{11} < 1.5V$ or $> 9V$

ELECTRICAL CHARACTERISTICS (Contd.)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Coincidence detector (ϕ_3)	11					
Output voltage typical range		0.5		6	V	
Output current:						
without coincidence			0.1		mAp–p	
with coincidence			0.5		mAp–p	
Phase comparison (ϕ_2: oscillator/ line flyback pulse)	5					
Control voltage range (typ)		5.4		7.6	V	
Control current			1		mAp–p	
Output resistance		High (see note 3)				$V_5 = 5.4V$ to $7.6V$
			8		kΩ	$V_5 < 5.4V$ or $> 7.6V$
Input current at blocked phase detector				5	μA	$V_5 = 5.4V$ to $7.6V$
Applications (see Fig. 4)	9					
Sync separator						
Input voltage (negative video signal)		1	3	7	Vp–p	
Input keying current range		5		100	μA	
Noise gating	10					
Input voltage		1	3	7	Vp–p	
Input keying current range		5		100	μA	
Superimposed noise voltage				7	Vp–p	
Vertical sync pulse separator						
Delay between leading edge of input and output signal, t_{on}			12		μs	
Delay between trailing edge of input and output signal, t_{off}				t_{on}	μs	
Output voltage	8		11		Vp–p	
Output resistance	8		2		kΩ	
Oscillator						
Frequency: free running			15.625		kHz	$C_{14} = 4.7nF$, $R_{15} = 10k\Omega$
Spread of frequency, $\Delta f_o/f_o$				±5	%	See note 5
Frequency control sensitivity, $\Delta f_o/\Delta I_{15}$			31		Hz/μA	
Adjustment range of network in Fig. 2			±10		%	
Influence of supply voltage on frequency $\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$				±0.05		See note 5, $V_1 = 12V$
Change of frequency when V_1 drops to 5V				±10	%	See note 5
Temperature coefficient of oscillator frequency per °C				$\pm 10^{-4}$		
Phase comparison (ϕ_1: sync pulse/oscillator)						
Control sensitivity			2		kHz/μs	
Catching and holding range (82kΩ between pins 13 and 15)			±780		Hz	$R_{13-15} = 82k\Omega$
Spread of catching and holding range			±10		%	See note 5
Phase comparison (ϕ_2: oscillator/ line flyback pulse)						
Permissible delay between leading edge of output pulse and leading edge of flyback pulse, Δtd		0		15	μs	
Static control error, td/td				0.2	%	
Overall phase relation See Note 6						
Phase relation between middle of sync pulse and the middle of the flyback pulse, t			2.6		μs	
Tolerance of phase relation Δt				0.7	μs	
Adjustment sensitivity of overall phase relation	5					
caused by: adjustment voltage $\Delta V_5/\Delta t$			0.1		V/μs	
adjustment current, $\Delta I_5/\Delta t$			30		μA/μs	

ELECTRICAL CHARACTERISTICS (Contd.)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Burst gating pulse						
Pulse width	7	3.7	4.0	4.3	µs	At 7V level
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse	7	2.15	2.65	3.15	µs	$V_7 = 7V$ At 7V level
Line drive pulse						
Output pulse duration, t_p	3	5.5	7.0	8.5	µs	$V_4 > 9.4V$
	3		$14 + t_d$		µs	$V_4 < 4V$, see note 7
Supply voltage for switching off the output pulse	1		4		V	
Internal gating pulse						
Pulse duration			7.5		µs	

NOTES
1. May also be left unconnected
2. VCR 'on' is normally achieved by connecting pins 11, via the VCR switch, to either ground or V_1
3. Current source
4. Emitter follower
5. Excluding external component tolerances
6. The adjustment of the overall phase relation and consequently the leading edge of the output pulse occurs automatically by phase detector 2 (See Fig. 2)
7. t_d = switch-off delay of line output stage.

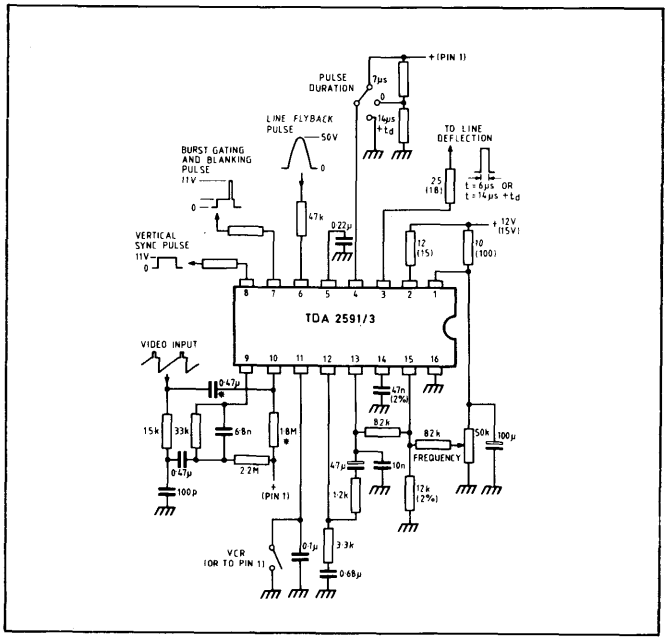

Fig. 4 Application and test circuit

PLESSEY
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TDA9503

LINE CIRCUIT FOR TV RECEIVERS

The TDA9503 is a monolithic integrated circuit for pulse separation and line synchronisation in TV receivers. The output stage of the TDA9503 (see Fig.2) supplies signals suitable for driving transistor line output stages.

An advanced version of the well-known type TBA950, the TDA9503 comprises the sync. separator with internal noise suppression, the frame pulse integrator, the phase comparator, a switching stage for automatic changeover of noise immunity and change of the slope of the phase control circuit, the line oscillator with frequency range limiter, a high-gain phase control circuit, a stage for generating the burst gate pulse in colour TV receivers, an undervoltage protection circuit and the output stage.

Due to the large scale of integration, or few external components are needed. The IC delivers prepared frame sync. pulses for triggering the frame oscillator. The phase comparator may be switched for video recording operation. A terminal (pin 14) for phase correction with the aid of the frame parabola is provided.

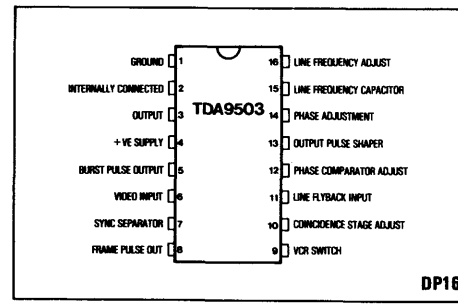


Fig.1 Pin connections (top view)

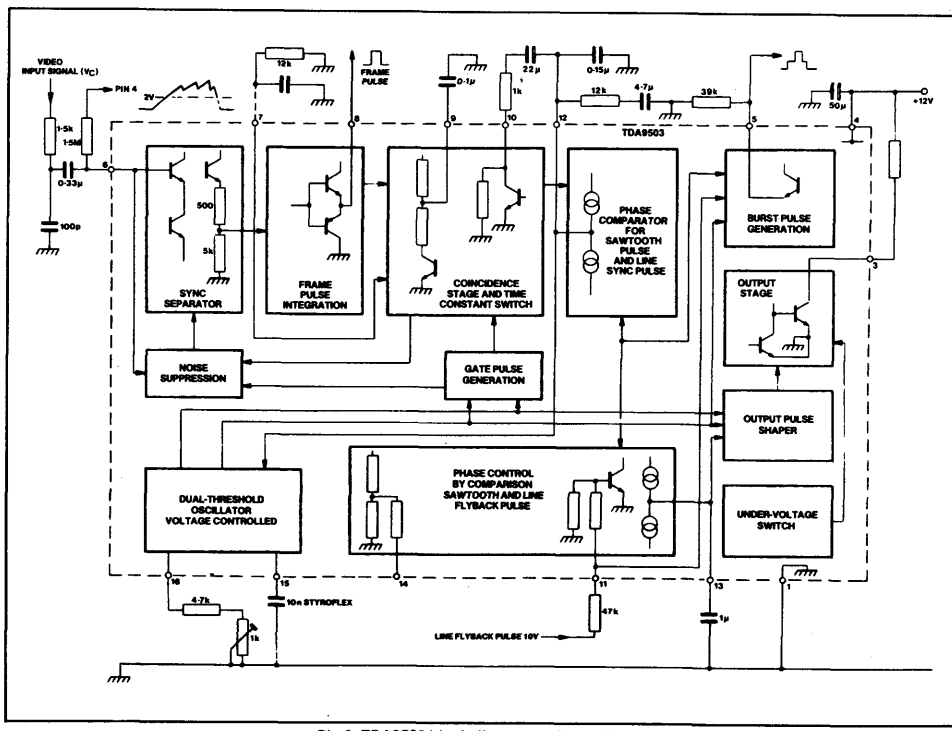


Fig.2 TDA9503 block diagram and test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

$V_4 = 12V$, $f_o = 15625\,Hz$, $T_A = 25°C$ in the test circuit Fig.2.

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	V_4	9		13	V	Pin 7 unloaded
Current consumption	I_4	—	38	45	mA	
Pin 7						
Amplitude of sync signal	V_7	9	—	—	V	
Output resistance (high level)	R_{A7}	—	500	—	Ω	
Threshold for frame pulses occurring at Pin 8	V_{7th}	—	2	—	V	
Pin 8						
Amplitude of the frame sync pulses	V_8	10	—	—	V	$I_8 = \pm 2mA$
Output resistance	R_{A8}	—	—	100	Ω	
Frame pulse duration	t_8	150	—	350	µs	Pin 7 unloaded
	t_8	300	—	650	µs	Pin 7 connected to ground via 1.2kΩ//0.33µF
Delay between leading edge of frame sync pulse at Pin 6 and output signal at Pin 8	t_{V8}	—	11	—	µs	Pin 7 unloaded
	t_{V8}	—	40	—	µs	Pin 7 connected to ground via 1.2kΩ//0.33µF
Pins 2 and 3						
Output transistor saturation voltage	$V_{3/1}$	—	—	0.5	V	220Ω from Pin 3 to +12V
Output pulse duration	t_3	23.5	26	28.5	µs	See Fig.3
Pin 5						
Burst gate pulse amplitude	V_{5B}	10	—	—	V	See Fig.3
Phase shift between centre of sync pulse and leading edge of burst gate pulse	t_{B1}	2.15	2.65	3.15	µs	
Burst gate pulse duration	t_5	3.7	4	4.3	µs	
Line blanking pulse amplitude	V_{5Z}	4	4.5	5	V	See Fig.3
Oscillator frequency	f_o	15625 ± 800			Hz	C15/1 = 10nF, R16/1 = 5.1kΩ
Frequency pull-in and holding range	$\pm\Delta f$	650	—	1200	Hz	
Slope of phase control loop	$\frac{t_d}{t_{SR}}$	100	—	—	—	
Slope of the phase comparator loop	$\frac{f}{t_{SR}}$	—	2	—	kHz/µs	
Phase shift between sync pulse of the video signal and the line flyback pulse	t_{SR}	2.1	2.6	3.1	µs	$t_d = 5\mu s$ (see Fig.3)

RECOMMENDED OPERATING CONDITIONS

	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_4	—	12	—	V
Input current during sync pulse	I_6	15	—	100	µA
Video signal input	V_6	1	3	6	V_{p-p}
Input switching current for internal noise suppression	I_{6s}	0.5	—	—	mA
Input current during line flyback pulse	I_{11}	0.1	—	2	mA
Switching current for VCR operation	I_9	2	—	—	mA
Input current (e.g. for frame parabola)	I_{14}	-50	—	50	µA
Ambient operating temp. range	T_A	0	—	60	°C

OPERATING NOTES

The sync separator separates the synchronising pulses from the composite colour video signal. The noise inverter circuit, which needs no external components, and an internal gate circuit free the sync signal from distortion.

The frame sync pulse is obtained by internal integration and limitation of the sync signal, and is available at pin 8. The typical delay time between the leading edge of the frame sync pulses at pin 6 and the output signal at pin 8 amounts to 11 µs. This time can be enlarged by means of an external RC combination connected to pin 7, which integrates the separated frame sync pulses, before they are given to the input of the following threshold switch. The latter has a threshold of 2V.

The frequency of the line oscillator is determined by a 10nF Styroflex capacitor at pin 15 which is charged and discharged periodically by two internal current sources. The external resistor at pin 16 defines the charging current and consequently in conjunction with the oscillator capacitor the line frequency.

The phase comparator compares the sawtooth voltage of the oscillator with the line sync pulse. Simultaneously an AFC voltage is generated which influences the oscillator frequency. A frequency range limiter restricts the frequency holding range.

The oscillator sawtooth voltage, which is in a fixed ratio to the line sync pulses, is compared with the line flyback pulse in the phase control circuit, in this way compensating all drift of delay times in driver and line output stage. The normal phase position is obtained if pin 14 is open-circuit. Any phase displacement can be corrected by a current or voltage fed into pin 14. The duration of the output pulse is thereby not influenced.

The burst gate pulse is derived from the sawtooth voltage of the line oscillator and therefore via the phase comparator synchronised with the line sync pulses of the colour video signal.

The switching stage has different functions. When the two signals supplied by the sync separator and the phase control circuit respectively are in synchronism a saturated transistor is in parallel with the integrated 2kΩ resistor at pin 10. Thus the time constant of the filter network at pin 12 increases and consequently reduces the pull-in range of the phase comparator circuit for the synchronised state. This arrangement ensures distrubance-free operation. Moreover, because the internal noise suppression and the internal gate circuit in synchronised operation are effective, the noise limitation is improved.

For video recording operation the automatic switchover can be blocked by a positive current fed into pin 9, e.g. via a resistor connected to pin 4. This reduces the time constant at pin 12 and increases the control current of the phase comparator thus steepening the static slope of the phase comparator which gives optimised matching in video recording operation.

The output transistor of the TDA9503 is operated in common emitter configuration. Its output current is limited to 50mA by the pull-up resistor between pin 3 and the supply voltage. This current serves for driving the line deflection driver transistor.

If the supply voltage goes down (e.g. by switching off the mains) a built-in protection circuit ensures defined line frequency pulses down to V_4= 4V and shuts off when V_4 falls below 4V, thus preventing pulses of undefined duration and frequency. Conversely, if the supply voltage rises, pulses defined in duration and frequency will appear at the output pin as soon as V_4 reaches 4.5V. In the range between V_4 = 4.5V and full supply voltage the shape and frequency of the output pulses are practically constant.

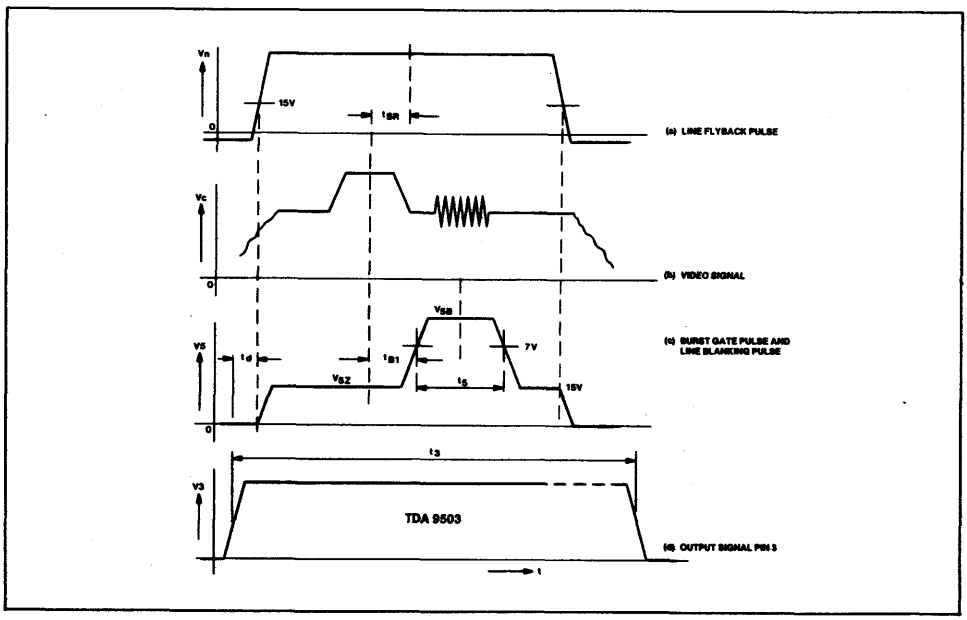


Fig.3 Phase relations

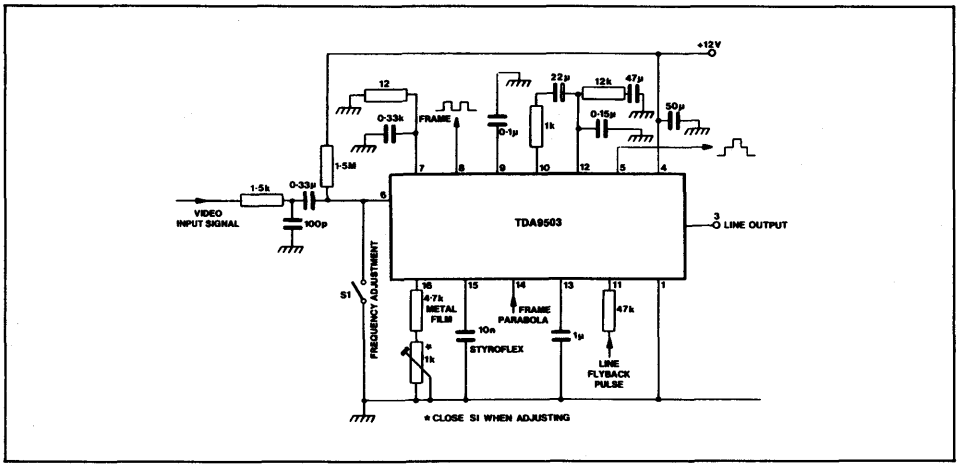
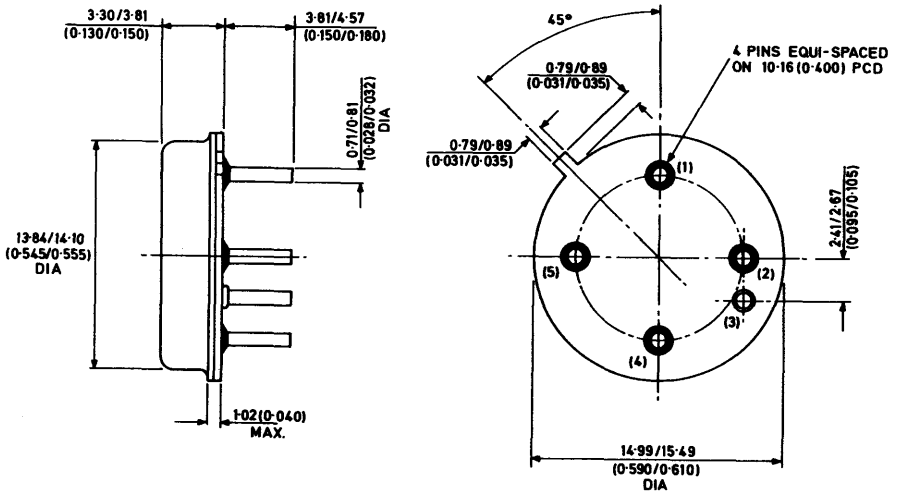


Fig.4 Operating circuit

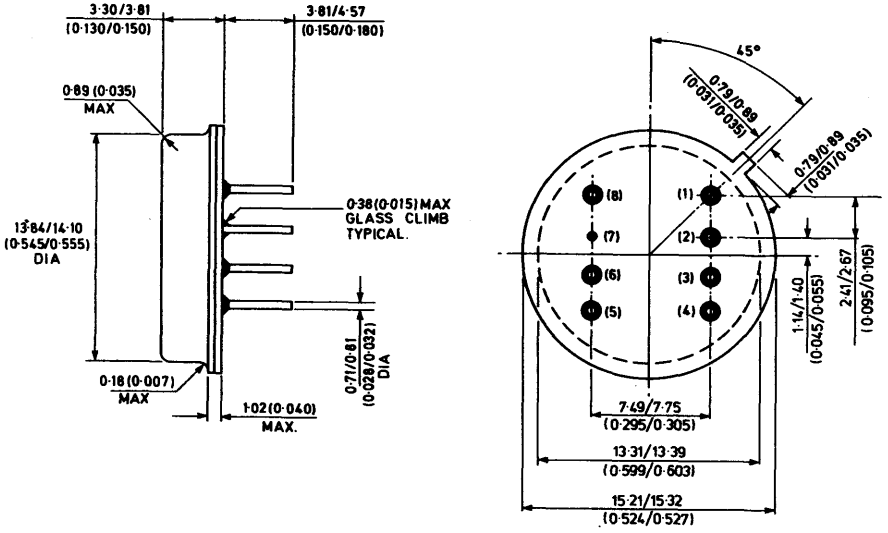
ABSOLUTE MAXIMUM RATINGS

	Symbol	Value	Unit
Supply voltage	V_4	14	V
Input voltage	V_6	-6	V
Output voltages	V_3	20	V
Output currents	I_5	-20	mA
	$\pm I_8$	20	mA
	I_3	50	mA
Input currents	I_{11}	5	mA
	I_9	5	mA
Operating temperature range	T_A	-10 to +60	°C
Storage temperature range	T_S	-55 to +125	°C

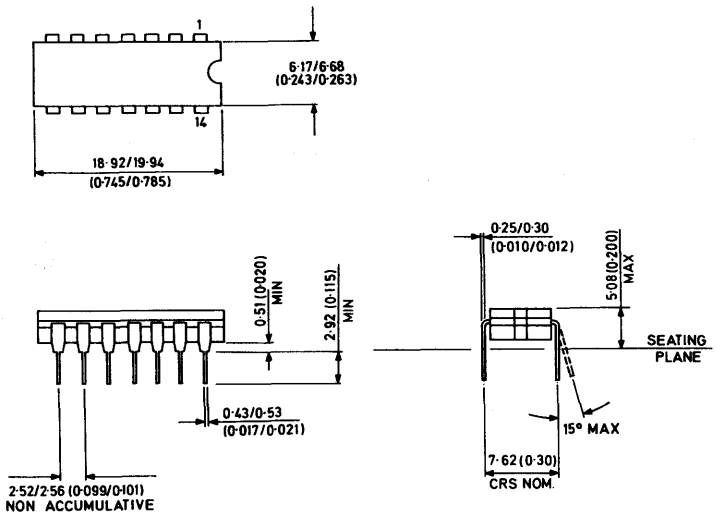
Package Outlines



5 LEAD TO 8 **CM5**

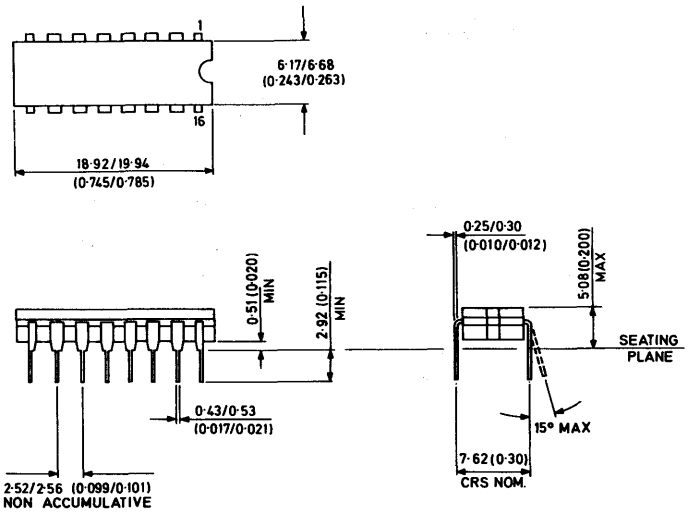


8 LEAD TO 8 **CM8**



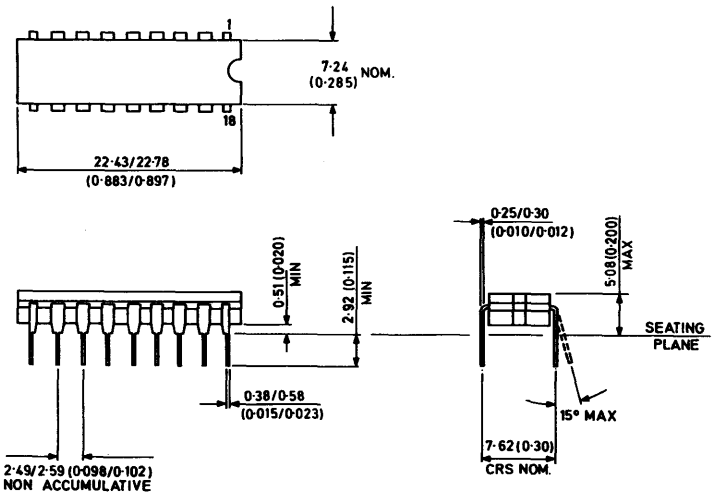
14 LEAD CERAMIC DIL

DG14



16 LEAD CERAMIC DIL

DG16



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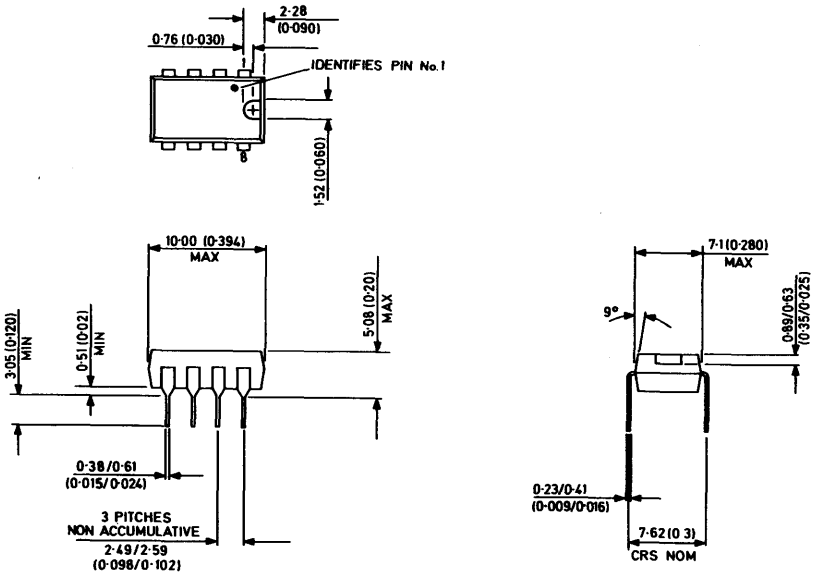
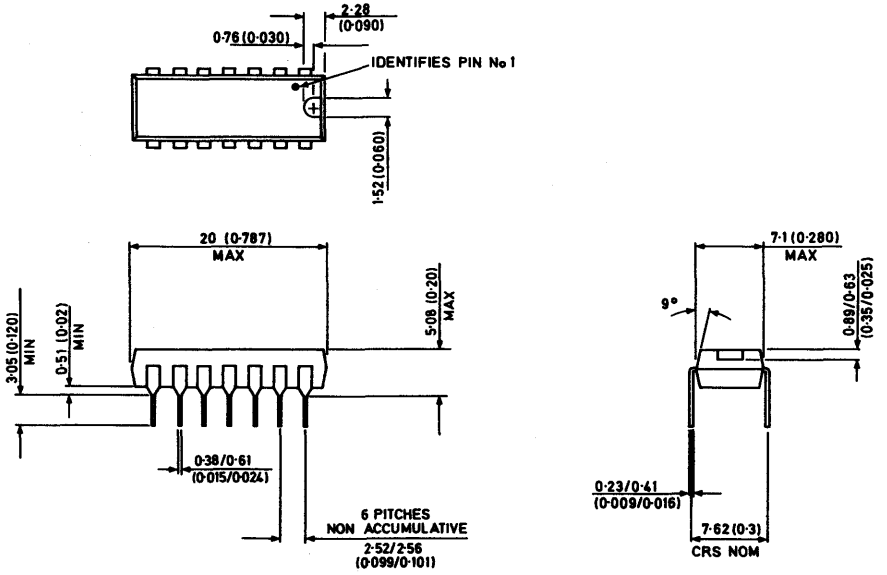


8 LEAD PLASTIC DIL

DP8



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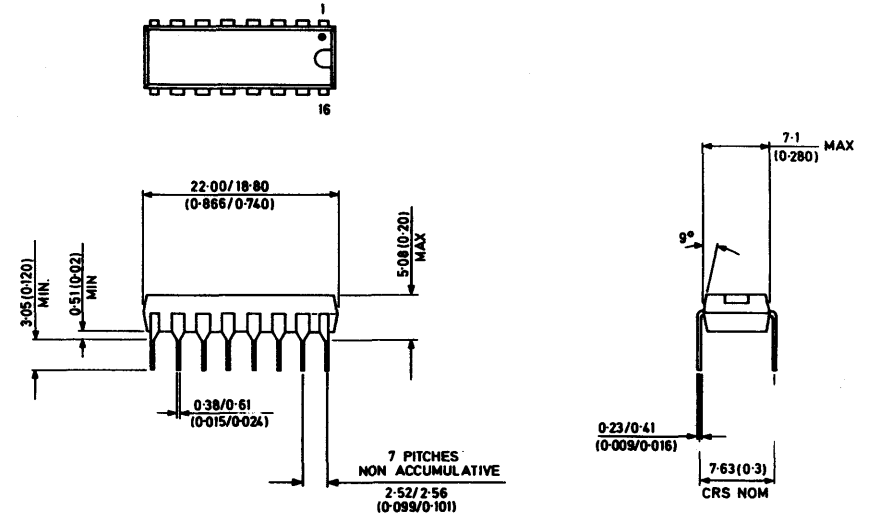

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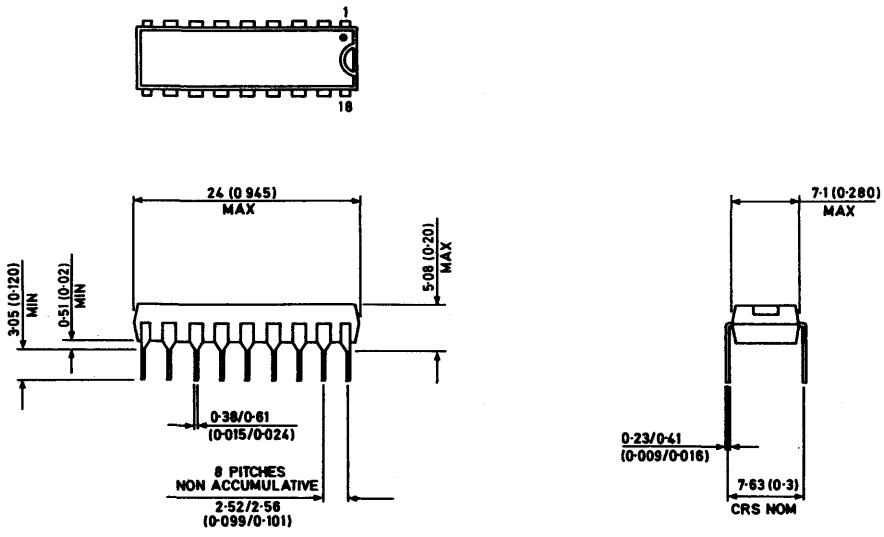

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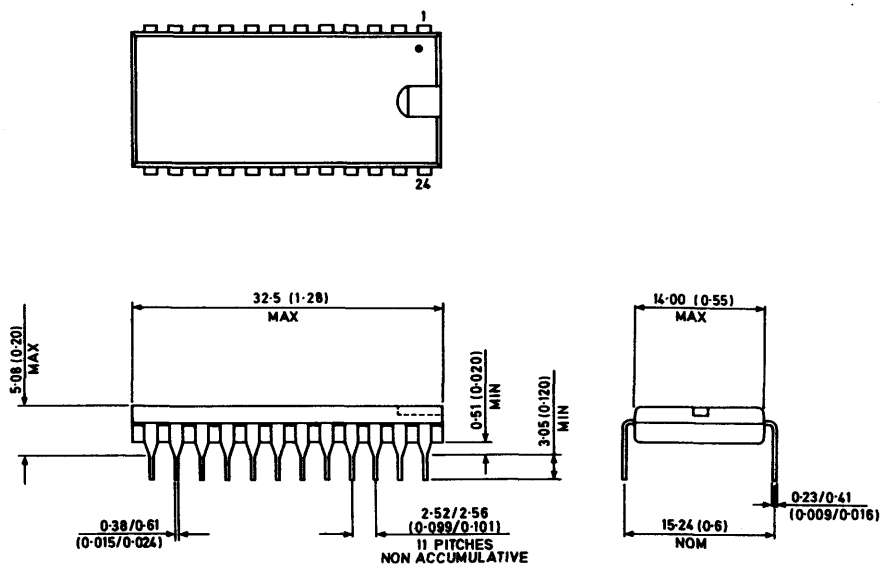

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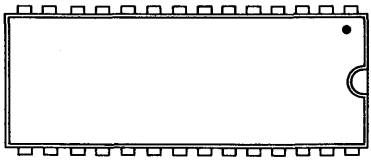
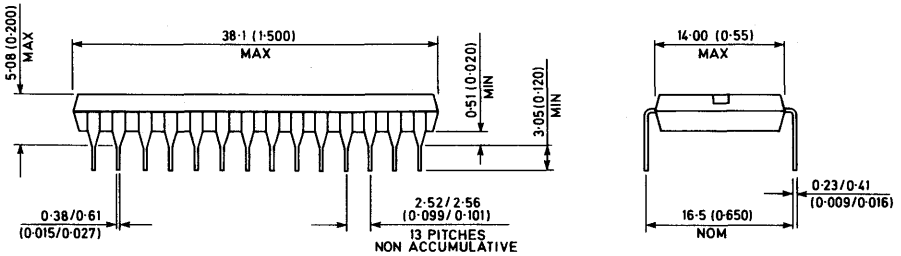
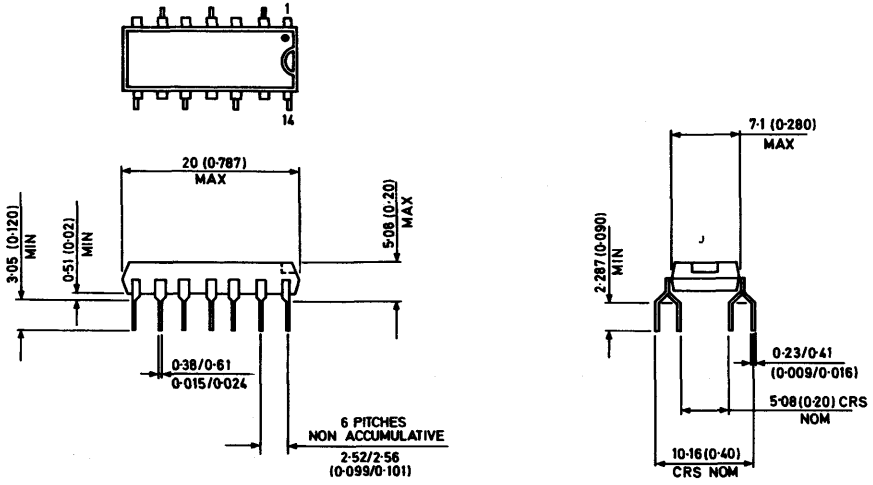




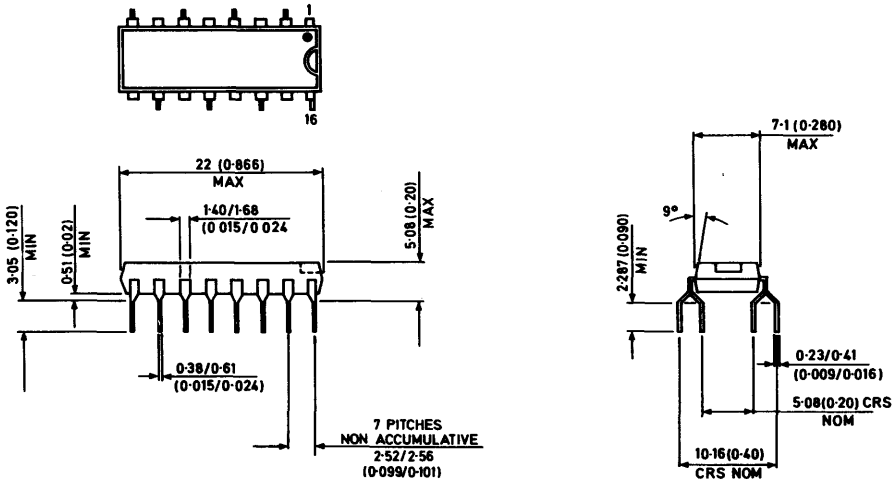
28 LEAD PLASTIC DIL

DP28



14 LEAD Q.I.L

QP14



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